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Feasibility study of a $Ge_2Sb_2Te_5$-clad silicon waveguide as a non-volatile optical on-off switch

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Abstract: This paper reports on the design optimization of compact optical ON-OFF switches based on a GST-clad silicon rib waveguide and compares it to a GST-clad silicon nanowire at the telecommunication wavelength 1.55 μm. Effective index and modal loss of the quasi-TE modes are calculated by a full-vectorial **H**-field finite element method. It shows that the electro-refraction effect-based switch may not be viable because of the higher modal loss in the GST crystalline state. On the other hand, the larger modal loss difference between GST amorphous and crystalline states would be more suitable for an electro-absorption type switch design. The effect of silicon slab thickness, silicon core width, and GST layer thickness for both the waveguides are presented. As the presence of the GST layer modifies the mode field profiles, so the incurring coupling loss at the butt-coupled junctions between the input/output silicon waveguide and Si-GST waveguide are also calculated by using the least squares boundary residual method. These results show that the GST-clad silicon rib waveguide with a 500-nm-wide silicon core, 60-90 nm thick silicon slab, and 15-25 nm thick GST layer is the optimal self-sustained switch design. In this case, a very compact, 2-5 μm long device is expected to show an extinction ratio of more than 20 dB with the total insertion loss of only 0.36 dB.

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1. Introduction

Miniaturization of photonic devices can have a significant contribution towards achieving the large-scale photonic integrated circuit (PIC). Over the past decade, silicon-on-insulator platform based photonic devices have shown considerable promise due to significant reduction in PICs size and power consumption along with their compatibility with the microelectronic circuits based on CMOS technology.

At present, two approaches are mostly used to design Si-based modulating and switching devices, which are carrier injection and carrier depletion. For carrier injection modulation, carriers are injected by forward biasing the PN junction. This type of the modulation is limited in speed by the recombination rate of the carriers and consume relatively high power. But, it has the advantage that it can allow large changes in the carrier density and therefore can achieve a higher modulation efficiency. On the other hand, carrier depletion, which modulates carrier density by reverse biasing the junction, is relatively fast and consumes less power as little current flows through the junction. However, it requires a higher overlap between the PN junction and the optical field, which leads to a larger insertion loss due to the initial doping of PN junction and lower modulation efficiency due to the small change in depletion width.

The phase change material (PCM), which provides a large difference in real and imaginary parts of refractive index between two stable and reversible states, can be used to mitigate some of

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these problems encountered by the free-carrier based modulators [1]. The phase change can be realized by laser irradiation, when the transformation can occur in a time scale of nanoseconds. In recent years, the scope for PCM has been expanded to oxides [1], such as vanadium dioxide (VO_2). The VO_2 is an electron material that has an insulator-metal phase transition at 68°C. Although VO_2 undergoes a large refractive index change during its phase transition, but losses in both the phases are high which makes the device volatile and also need continuous power to maintain each state [2].

Several electro-optic devices based on the phase change material $Ge_2Sb_2Te_5$, commonly known as GST, have been reported to have better optical performance than the VO_2 [3,4]. These devices utilize high differential refractive index between the amorphous and crystalline states of GST to yield a more compact electro-optic device. The phase change of the GST can be thermally [5], optically [6], or electrically [7] induced and thus can potentially operate at an ultrahigh speed. For thermally driven device, crystallization is achieved by heating GST above the transition temperature and then slowly cooling down. Re-amorphourization is achieved by heating the crystalline GST above the melting point followed by rapid cooling [8]. In addition to that, unlike other electro-optic materials, GST possesses the self-holding feature, which means it requires energy only to switch from one state to another, but continuous supply of energy is not needed to maintain a given state. A recent work also reports on the practical implementation of asymmetric Mach-Zehnder switch using GST clad silicon rib waveguide [9].

In this paper, we focus on the design optimization of a compact electro-optic ON-OFF switch based on a GST-clad silicon rib waveguide and a GST-clad silicon nanowire waveguide at the telecommunication wavelength 1.55 μm is presented. Here, a rigorous **H**-field based full-vectorial finite-element method (VFEM) in conjunction with the perturbation technique is used to find the complex modal indices with the variations of the waveguide width and height of different layers. Following that, the least squares boundary residual (LSBR) method, a rigorous junction analysis approach, is used to calculate the coupling loss at the butt-coupled junctions to determine the optimal waveguide parameters in order to achieve a lower insertion loss and a higher extinction ratio of a self-sustained switch.

2. Theory and design method

Figure 1(a) shows the three-dimensional view of an optical switch based on a Si-GST rib waveguide, identified here as WG1. Here, outer two waveguide sections are passive, while the central section is active. The active section consists of a standard single-mode silicon rib waveguide with a GST top-clad layer. The cross-sectional view of the active section is shown in Fig. 1(b). Here, the thickness of the silicon core is identified as H, its width is taken as W, and the slab layer thickness is taken as S. The GST patch thickness is taken as T on the top and B at the sides, as it has been observed that thickness at the sides are often only 40% of that in the top. The length of GST section, deposited on top of the silicon rib waveguide to form the hybrid waveguide for optical switching, is taken at L_{GST}.

It should be noted that, if the waveguide is etched fully ($S = 0$ nm), then this represents a standard silicon nanowire waveguide (NW), identified here as WG2. The WG2 with its width W and height H can also be wrapped with a GST clad layer with thickness T. Both these Si waveguide structures will be evaluated through numerical simulations and comparison will be made for better design optimization of the optical switches.

2.1. Modal analysis method

For all practical optical waveguides with 2-D confinement, their eigenmodes are classified as quasi-TE and quasi-TM modes, as they contain all the six components of the **E** and **H** fields. The full-vectorial **H**-field based finite element method, which is one of the most accurate and numerically efficient approaches, is used here for modal analyses [10]. The functional of the

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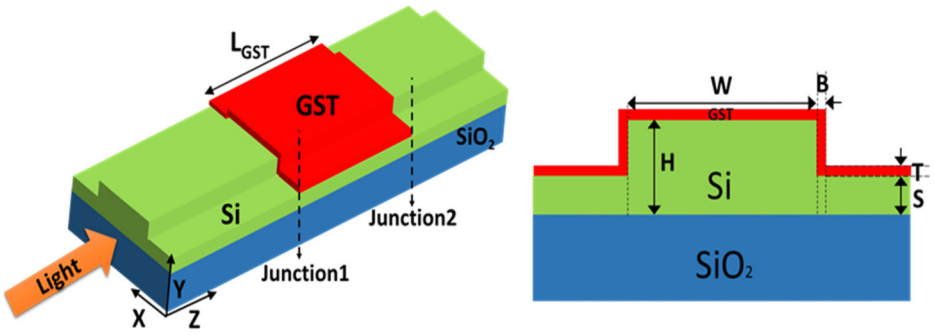

Fig. 1. (a) Schematic of the optical switch (WG1 based), (b) Cross-sectional view of the coupled section WG1.

vectorial H-field finite element formulation with the penalty term can be given as:

$$\omega^2 = \frac{\int[(\nabla \times H)^* \cdot \varepsilon^{-1} \cdot (\nabla \times H)dxdy + \rho(\nabla \times H)^* \cdot (\nabla \times H)]dxdy}{\int H^* \cdot \mu \cdot Hdxdy} \quad (1)$$

where, **H** is the full-vectorial magnetic field, * denotes a complex conjugate and transpose, ω^2 is the eigenvalue, ω is the angular frequency of the wave, ϵ and μ are the permittivity and permeability, respectively, and ρ is a weighting factor for penalty term.

As the WG1 and WG2 waveguides contain a layer of GST cap with complex refractive index, so modal loss is induced. However, most of the formulations used in FEM, such as the **H**-field formulation are often restricted to structures without modal loss or gain. For most practical waveguides, loss or gain values could be small, and the imaginary part of the complex propagation constant is small compared to the real part. In this case, the full-vectorial **H**-field finite element method in conjunction with the perturbation technique [11] will be a more suitable approach to calculate the modal loss values of these GST clad waveguides.

2.2. Calculation of coupling loss at the Si and Si-GST waveguide junctions

It is desirable to have a lower coupling loss at the junction interface for both the GST states. A powerful numerical approach, the LSBR method, is utilized to calculate the power coupling between the input silicon waveguide and the active Si-GST waveguide. To undertake the analyses, a full-vertorial FEM is used to obtain the modal field profiles over the cross-section at the both sides of a discontinuity interface. Following that, the LSBR method [12] is used for calculating the power transfer efficiency by enforcing the continuity of the tangential **E** and **H** fields at the junction interface to obtain the transmission and reflection coefficients of the fully hybrid modes at the discontinuity interface.

3. Numerical results

3.1. Refractive index of the material for simulation

In this work, the refractive indices of silicon and silica at operating wavelength at 1.55 μm are taken as n (Si) = 3.481, n (SiO_2) = 1.44468. The complex refractive indices of GST, measured by using the VASE ellipsometer, are taken as n (Amorphous-GST) = 4.03654 + j0.03746, n (Crystalline-GST) = 6.49615 + j1.0655, respectively [9,13].

3.2. Fundamental mode field profiles

In this paper, both for the VFEM and LSBR approaches, in-house codes, are used for numerical simulations. For the quasi-TE mode, H_y is the dominant and H_x and H_z are the non-dominant

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components of the magnetic field, **H**. At first, the input silicon rib waveguide with W = 500 nm, H = 220 nm, S = 90 nm is simulated, and the H_y field profile of the quasi-TE H_y^{11} modes of this waveguide is shown in Fig. 2(a). It can be observed that its field is confined in the silicon rib core and extends slightly to the upper air and lower silica buffer regions. It also extends a bit laterally into the lower slab region. The mode effective index ($n_e = \beta/k_0$) is calculated as 2.5319 for the passive input waveguide. Here, β is the propagation constant and k_0 is the free-space wavenumber. Additionally, variation of the H_y component of the H_y^{11} mode along the vertical directions is shown in Fig. 2(b). The silica buffer region is shown by a blue shade and silicon region with a light green shade and a dashed line inside shows the interface between the rib and slab region. Here, it can be noted that, the maximum H_y component value is inside the rib and near to the interface between the silicon rib and slab. The H_y field decays exponentially both in upper clad air region and lower SiO_2 substrate region. As the decay in the lower substrate is slower so H_y value at this interface is slightly higher than that at the Si/air interface.

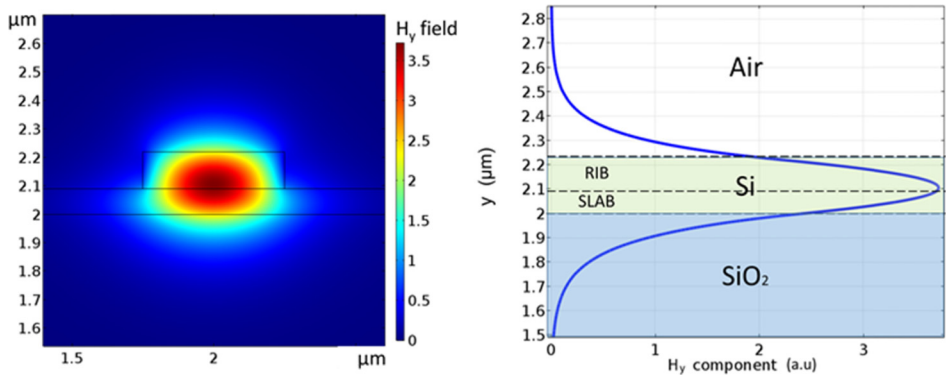

Fig. 2. (a) H_y field profile, (b) H_y variation along the vertical direction, for input silicon rib waveguide with W = 500 nm, H = 220 nm, and S = 90 nm.

Subsequently, an ultra-thin GST layer is deposited on top of the silicon rib waveguide to form a hybrid waveguide (WG1) for optical switching. Although GST states can be changed by optical, electrical and thermal approaches, however, in our switch design, we have assumed that the state of the GST is changed from its initial amorphous to the crystalline state by thermal annealing. This crystallization can be achieved by heating GST above the glass transition temperature and then slowly cooling down [9].

The H_y field of the H_y^{11} mode of WG1 in the amorphous state is shown in the Fig. 3(a). It shows that when the GST is in the amorphous state, the guided mode is more confined in the middle of silicon rib region and slightly extends to the top GST layer and air which is similar like Fig. 2(a). Variation of H_y along the y-axis at the center of the waveguide is shown in Fig. 3(b). The GST layer is shown by a pink shade and silicon region with a light green shade and a dashed line inside shows the separation between the rib and the upper Si slab. It can be observed that the maximum H_y value is inside the silicon rib but shifts a little upward than that in Fig. 2(b).

However, when the GST is switched to a crystalline state, its refractive index is increased considerably, and the Hy field profile of the Hy11 mode of WG1 in crystalline state is shown in Fig. 4(a). It can be observed that although the field is confined well in the silicon rib layer, but a small amount of modal field is also extended to the top GST layer. It suggests that when the GST turns to crystalline state, more power is confined into the GST layer. The Hy field profile along the vertical direction is shown in Fig. 4(b). It can be noted that in the crystalline state, the maximum Hy value is still inside the silicon rib layer but closer to the interface between the silicon rib and the top GST layer. Compared to the GST in amorphous state shown in Fig. 3(b), a

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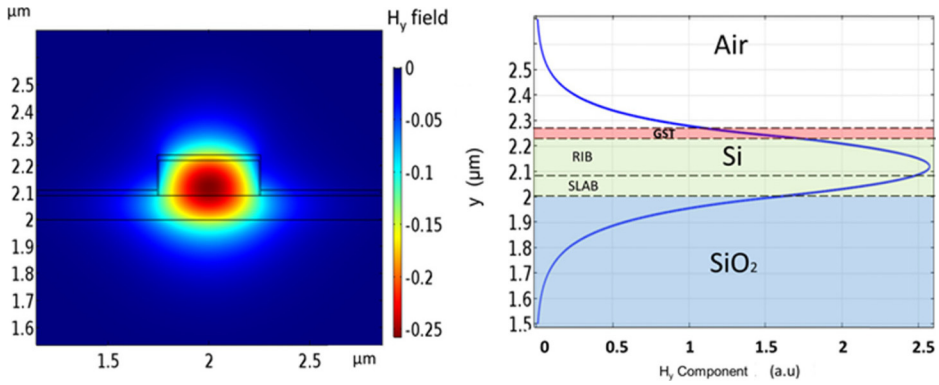

Fig. 3. (a) H_y field profiles, (b) H_y variation along the vertical direction, for WG1 in amorphous state with W = 500 nm, H = 220 nm, S = 90 nm, T = 20 nm.

larger modal field is presented in the top silicon rib region and less into the Si slab region when the GST is in the crystalline state.

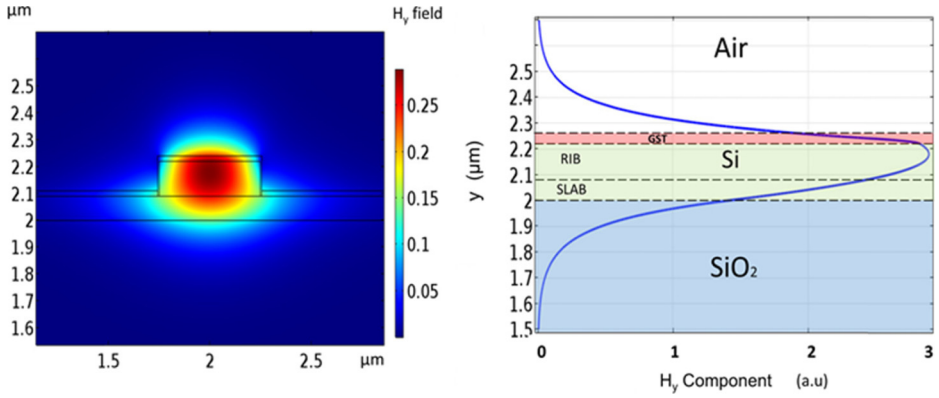

Fig. 4. (a) H_y field profiles, (b) H_y variation along the vertical direction, for WG1 in crystalline state with W = 500 nm, H = 220 nm, S = 90 nm, T = 20 nm.

3.3. Modal solution characteristics

Following the modal analysis, when the GST in amorphous state, the mode effective index of WG1 is written as ($n_{e1} + j*k_{e1}$), and while in crystalline state this is written as ($n_{e2} + j*k_{e2}$). The mode absorption loss α of the waveguide in dB per micrometer for each state, can be calculated from the imaginary part of their effective indices k_e, as:

$$\alpha = 4.343 \times \left(\frac{4\pi k_e}{\lambda}\right) \tag{2}$$

The calculated modal solution parameters for the $H_y{}^{11}$ mode of WG1 (W = 500 nm, S = 90 nm, T = 20 nm and B = 8 nm) are given in Table 1. It can be noted that when GST is in crystalline state, the waveguide has a larger effective index, both in real and imaginary parts, which also suggests a larger mode loss. The WG1 here has a strong electro-refraction ER = (n_{e2}-n_{e1}) = 0.2614 and also a strong electro-absorption EA = (k_{e2}-k_{e1}) = 0.1811, because there are significant changes in both real and imaginary parts of GST refractive indices induced by the phase change. Electro-refraction,

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which considers the differential real part of the effective index, is widely used to design optical switches. The optical switch can be comprised of either a Mach-Zehnder interferometer (MZI) with two branches or a directional coupler incorporating two adjacent waveguides. However, sometimes ER-based devices need additional requirements like ER>>EA. For a MZ-based switch, we would prefer a higher ER values for a compact device but also prefer lower loss values for both the states. On the other hand, the Electro-absorption effect also can be utilized for modulation, where the differential mode loss between the two states is exploited to achieve the optical switching.

Table 1. Modal solution characteristics

	n_e	k_e	Mode loss α (dB/μm)
Amorphous	2.6768	0.0029	0.1036
Crystalline	2.9382	0.1841	6.4811
Difference	0.2614	0.1811	6.3775

In the following sections, variations of both ER and EA characteristics of the WG1 with waveguide width and height of different layers are thoroughly investigated. Similar results for the WG2, a standard silicon nanowire waveguide (NW), are also shown later for comparison.

Variations of the real part of the effective index with the slab height, S, are shown in Fig. 5. Results for amorphous state (AM) are shown by blue lines and similarly those for the crystalline state (CR) are shown by red lines. The results for W = 500 nm are shown by solid lines with solid symbols and those for a narrower W = 450 nm are shown by dashed lines with hollow symbols. When GST is in amorphous state, it can be observed that for W = 500 nm and T = 20 nm, shown by a solid blue line, the n_{e1} increases with slab thickness S as the waveguide core area increases. However, it should be noted that the modal confinement in the rib core will reduce as more field will extend to the slab region. On the other hand, the real part of the effective index for the crystalline state shown by a solid red line, also increases with S, but with higher values than the amorphous state's values. This is because, when the GST is in crystalline state, its refractive index is 1.5 times larger than that of the amorphous state so that the WG1 will have higher effective index values for the crystalline state. When the W reduces to 450 nm, the real effective index of WG1 for both the states, shown by the dashed red and blue lines are lower than that for W = 500 nm. It can be concluded that the wider silicon waveguide will have higher ne values for both the states when the slab height S increases from 10 to 120 nm.

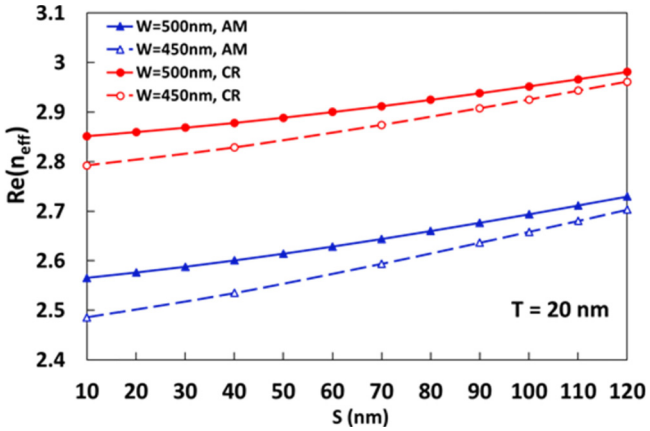

Fig. 5. Variations of the real part of effective indices of WG1 in amorphous and crystalline states with the slab height, S, for two different widths.

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Next, effect of GST thickness T on the modal solutions is studied. Here, we have considered a fixed width, W = 500 nm and for WG1, the slab height is kept fixed at S = 90 nm. In Fig. 6, the real effective index of WG1 for amorphous state n_{e1} is shown by a solid blue line. When the GST thickness T increases from 10 to 30 nm, the n_{e1} also increases slowly from 2.607 to 2.743. On the other hand, the real effective index for the crystalline state n_{e2}, shown by a solid red line, increases more rapidly from 2.73 to 3.16, compared to its amorphous state. When the waveguide is changed to a silicon nanowire waveguide (i.e. S = 0), the real effective index of WG2 for both the states are shown by the dashed red and blue lines for comparison. It can be concluded that the silicon rib waveguide, WG1 have higher n_e values for both the states when the GST thickness T increases from 10 to 30 nm.

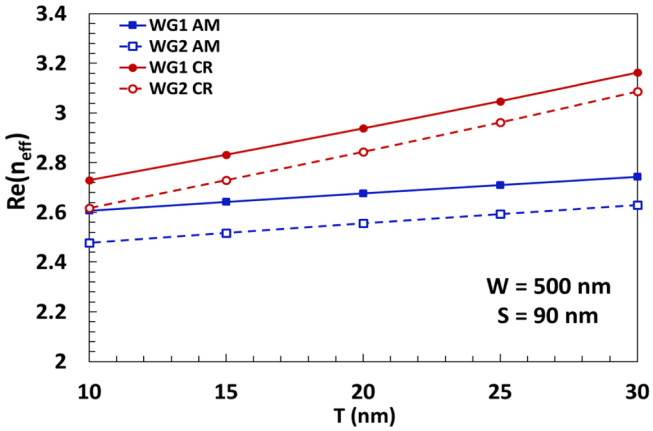

Fig. 6. Variations of the real part of effective indices for amorphous and crystalline states with the GST thickness, T, for WG1 and WG2.

In switches, the phase change $\Delta\varphi$ is the product of the differential propagation constant $\Delta\beta$ and the device length L, which affects the transfer of light from the input guide to the output guide. Here, $\Delta\varphi$ is given as:

$$\Delta\varphi = \Delta\beta L = \left(\frac{2\pi}{\lambda}\right) \cdot \Delta n_e \cdot L = \left(\frac{2\pi}{\lambda}\right) \cdot (n_{e2} - n_{e1}) \cdot L = \left(\frac{2\pi}{\lambda}\right) \cdot ER \cdot L \tag{3}$$

If the Mach-Zehnder interferometer (MZI) is used for switch geometry, the value of "$\Delta\varphi$" needs to be π rad, and the length of such switches is given as:

$$L_\pi = \frac{\pi}{\Delta\beta} = \frac{\lambda}{2 \cdot \Delta n_e} = \frac{\lambda}{2 \cdot (n_{e2} - n_{e1})} = \frac{\lambda}{2 \cdot ER} \tag{4}$$

Next, effects of the waveguide parameters, on the ER and MZI active waveguide length, L_π are studied. In Fig. 7, when W is set at 500 nm and GST height T at 20 nm, the ER (n_{e2}-n_{e1}) of WG1 between amorphous and crystalline states is shown by a solid red line using the left-hand side scale. With the steady increase of slab height S from 10 to 120 nm, the ER shows an opposite trend, which is reducing from 0.286 to 0.252. The L_π of the WG1 is shown by a solid blue line using the right-hand side scale. The L_π of the WG1 increases gradually from 2.71 to 3.08 μm, as slab thickness S is increased. When the W reduces to 450 nm, the ER shown by a dashed red line (left scale) also reduces, but these values are always higher than the solid line, which was for width W = 500 nm and their differences become smaller with the increasing S.

On the other hand, the L_π of the 450 nm wide waveguide, shown by a dashed blue line using the right-hand side scale, also increases, but this is always lower than the solid line shown for W = 500 nm and their differences become smaller with the higher S.

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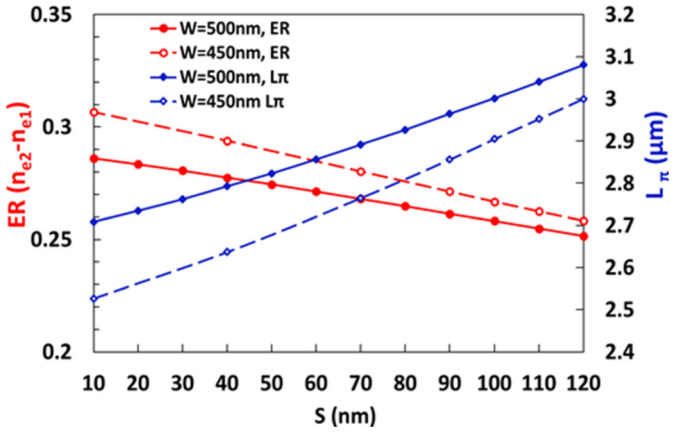

Fig. 7. Variations of the ER and L_π of WG1 between the amorphous and crystalline states with Si slab height, S.

In Fig. 8, we have considered a fixed width of W = 500 nm, and for WG1 the slab height S is also kept fixed at 90 nm. Variations of ER (Δn_e) are shown by red lines, using the left-hand side scale, while the L_π variations are shown by blue lines using the right-hand side scale. It can be observed, the variation of ER for the WG1 shown by a solid red line increases with the GST thickness T. When the waveguide core is changed to silicon nanowire waveguide (NW), the ER of WG2 is shown by a dashed red line, where it can be observed that NW WG2 can achieve a slightly higher ER and their differences also increase when the T increases steadily from 10 to 30 nm.

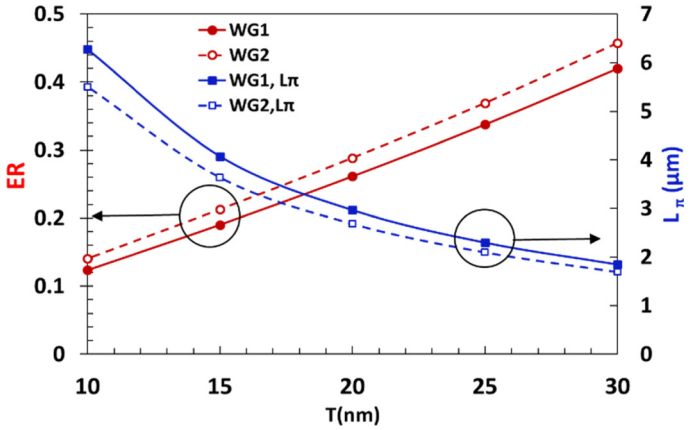

Fig. 8. Variations of the ER and L_π between amorphous and crystalline states with GST thickness T for WG1 and WG2.

On the other hand, variation of L_π for the WG1 shown by a solid blue line decreases with the GST thickness T. The L_π of the WG1 rapidly decreases from a higher value of 6.27 μm to a lower value of 1.85 μm when T is increased from 10 nm to 30 nm. Variation of the L_π of the WG2 is shown by a dashed blue line, which also decreases with T but with lower values compared to that of the WG1. It can be concluded that the silicon rib waveguide WG1 will have longer L_π and their difference between two waveguides becomes smaller when T increases steady from 10 to 30 nm. It is clearly shown here, GST thickness is the most critical parameter in the design of

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optical switches. A very compact device of 2-6 μm long is feasible by using either a silicon rib or a nanowire waveguide.

As GST introduces material loss, so next the variations of modal loss for these two states with the slab thickness S are shown in Fig. 9. Results for the amorphous state (AM) are shown by blue lines, using the left-hand side scale, while those for the crystalline state (CR) are shown by red lines using the right-hand side scale. The results for W = 500 nm are shown by solid lines with solid symbols and those for W = 450 nm are shown by dashed lines with hollow symbols. When GST is in amorphous state, it can be observed that for W = 500 nm and T = 20 nm, shown by a solid blue line, the mode loss decreases with the slab thickness S, as the waveguide core area increases. On the other hand, the mode loss for the crystalline state, shown by a solid red line, also decreases with S, but these values are nearly two orders of magnitude larger than those in the amorphous state. This is because, for the GST in the crystalline state, imaginary part of its refractive index is much larger than that in the amorphous state. When the W reduces to 450 nm, the mode loss of WG1 for both the states, shown by the dashed red and blue lines, increases. It can be concluded that a wider silicon waveguide can yield smaller mode loss values for both the states when the slab thickness S increases steady from 10 to 120 nm.

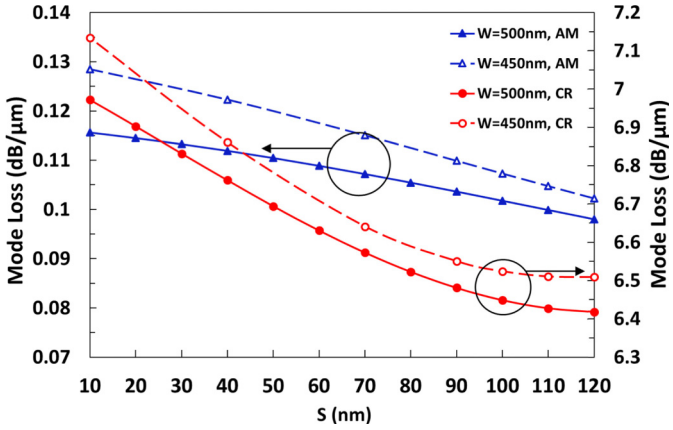

Fig. 9. Variations of mode loss of WG1 in amorphous and crystalline states with S of two different values of W.

Moreover, when W is kept fixed at 500 nm and S at 90 nm, a steady increase of GST thickness T from 10 to 30 nm leads to large increase in the mode loss values of WG1 in both amorphous and crystalline states. However, when the WG1 is changed to a silicon nanowire core WG2, it will have a larger mode loss in both amorphous and crystalline states. However, these are not shown here, but total device losses for both the states are shown below.

Variations of the total modal loss ($L_\pi * \alpha_1$) of WG1 with the slab thickness, S, for device length = L_π, W = 500 nm and T = 20 nm for the amorphous state is shown by a solid red line in Fig. 10. With the steady increase of silicon slab height S from 10 to 120 nm, the total loss value reduces slightly from 0.313 to 0.302 dB. On the other hand, the total modal loss for the crystalline state ($L_\pi * \alpha_2$) shown by a blue solid line increases slightly from 18.89 to 19.77 dB with the slab height. These values are much higher than those in the amorphous state. When the width W reduces to 450 nm, the total modal loss of WG1 for both the states are shown by the two dashed lines. It can be concluded that the wider silicon waveguide core can achieve a smaller total modal loss for amorphous state and larger loss values in crystalline state while the slab height S increases from 10 to 120 nm. Although the smaller L_π may yield a possible compact MZI switch with a lower total modal loss in the amorphous state for both the WG1 and WG2

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designs, but 18-20 dB modal loss for the crystalline states will cause incomplete interference and thus a poor switching extinction ratio.

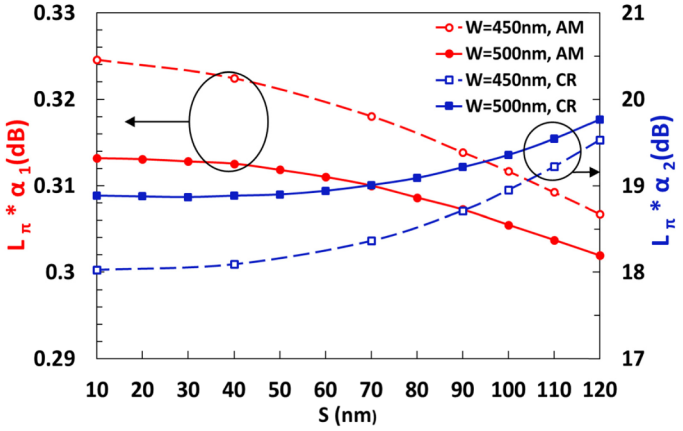

Fig. 10. Total modal loss of WG1 in amorphous and crystalline states with varying S for two different widths.

As it is clear from the above discussion that the ER based approach is not suitable for a possible GST switch, next the EA (k_{e2}-k_{e1}) effect will be considered for the possible switch design. Here, we assume that the switch has a total extinction ratio of 20 dB between amorphous and crystalline states, which means only 1% power at the "OFF" state compared to the "ON" state. However, any other preferred extinction ratio can also be considered. In this particular case, the corresponding device length L_b can be calculated as:

$$L_b(\mu m) = \frac{20}{(\Delta\alpha)} = \frac{20}{(\alpha_2 - \alpha_1)} \tag{5}$$

If we consider a GST-clad section of length L_b, then the modal loss for the crystalline state would be 20 dB higher than that of the amorphous state.

Variations of switch length L_b and modal loss of amorphous state (L_b*α_1) with the slab height S are shown in Fig. 11. When W is fixed at 500 nm and T = 20 nm, the switch length L_b is shown by a solid red line. With the steady increase of S from 10 to 120 nm, the switch length L_b increases monotonically from 2.92 to 3.16 μm, which also shows that a novel compact optical switch is possible. For W = 450 nm, it can be noticed that the L_b also increases but these values are always smaller than that of a wider waveguide. On the other hand, total modal loss of the device for a low-loss "ON" state is shown by blue lines on the right scale. For the W = 500 nm, the total modal loss of the amorphous state shown by a solid blue line reduces from 0.34 to 0.31 dB when S increases to 120 nm. Similarly, for W = 450 nm shown as a dashed blue line, the total loss also reduces but always has larger loss values than those of the 500-nm-wide waveguide. It can be concluded here, a lower slab thickness S can yield a shorter switch, but the total modal loss for "ON" state would be higher. However, a Figure-of-Merit, could be their product remains almost constant. Similarly, a narrower silicon width W not only requires a longer device length but also suffers from a larger modal loss, which is thus may not be a preferred design.

Variations of the device length and total modal loss in amorphous state with the GST thickness, T are shown in the Fig. 12. In this case, when W is fixed at 500 nm and S = 90 nm, the device length L_b's of WG1 and WG2 are shown by a solid red line and a dashed red line, respectively, using the left-hand side scale. It can be noted that when the GST thickness, T increases from 10 to 30 nm, modal loss for crystalline state reduces rapidly, but not shown here. But as a result, the device length L_b for both WG1 and WG2 decrease from 7 μm to a lower 2 μm value to achieve

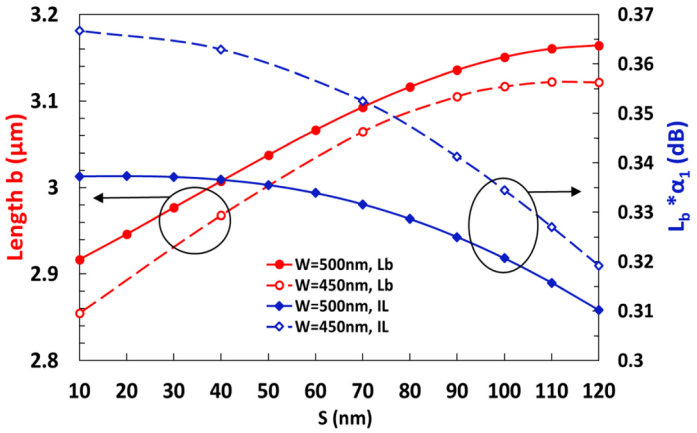

Fig. 11. Lb and total modal loss of WG1 in amorphous state with varying S for two different W.

20 dB differential loss, as shown here by red lines. However, L_b of WG1 with a rib structure always needs to be slightly longer, but their difference will become smaller as the T increases to 30 nm. On the other hand, the total modal loss for amorphous state of WG1 and WG2 is shown by blue solid and dashed lines using the right-hand side scale. It can be noted that, the propagation loss of WG1 decreases from 0.39 to 0.27 dB as the T increases to 30 nm, meanwhile the loss of WG2 also decreases but always suffers from higher loss values than that of WG1. It can be concluded that with a larger GST thickness T, the WG1 with the rib structure yields a short device length and also smaller loss for the 'ON' state. On the other hand, the adoption of a silicon nanowire waveguide WG2, shown by dashed lines, yields a slightly shorter device but with a slightly larger total loss.

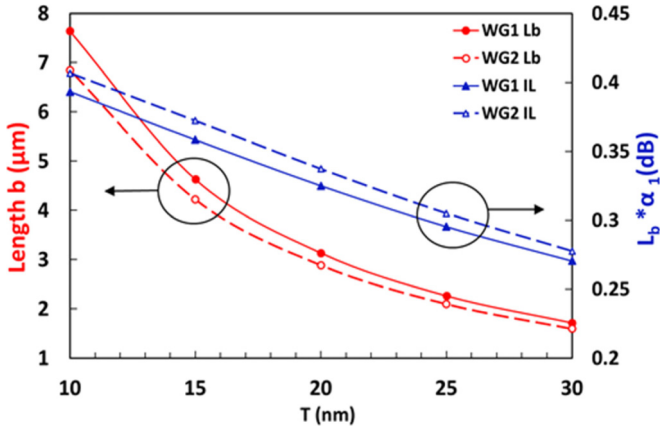

Fig. 12. L_b and total modal loss in amorphous state with varying T for WG1 and WG2.

The modal field profiles for the incident silicon rib waveguide and GST-cladded silicon rib waveguide at crystalline states were shown in Figs. 2 and 4. These field profiles were different due to the presence of GST layer and particularly very different for the crystalline GST state. This indicates the possibility of a considerable power loss at junctions 1 and 2. The performance of GST switches may be critically affected by these coupling losses and considered next.

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The effect of slab thickness S on the junction loss is first studied. In this case, the width W is fixed at 500 nm and T = 20 nm, the total junction losses of WG1 from both the input and output side coupling, calculated by the LSBR method for the amorphous state, are shown by a solid red line in Fig. 13. It shows that when the slab thickness S increases from 10 to 120 nm, the total junction losses can decrease from a larger value of 0.115 dB at S = 10 nm, and then reach a nearly constant level around 0.04 dB for slab thickness S larger than 60 nm. On the other hand, the total junction loss of WG1 in crystalline state is shown by a solid blue line using the right-hand side scale. This junction loss reduces from 0.98 dB to the minimum 0.475 dB when the S increases to 70 nm. It then increases rapidly to a large value of 1.21 dB at S = 120 nm. This suggests that slab thickness, S between 60-90 nm, can yield a satisfactory design with a lower junction loss at the amorphous "ON" state, as additional coupling loss in the crystalline state may not be that critical as being the "OFF" state.

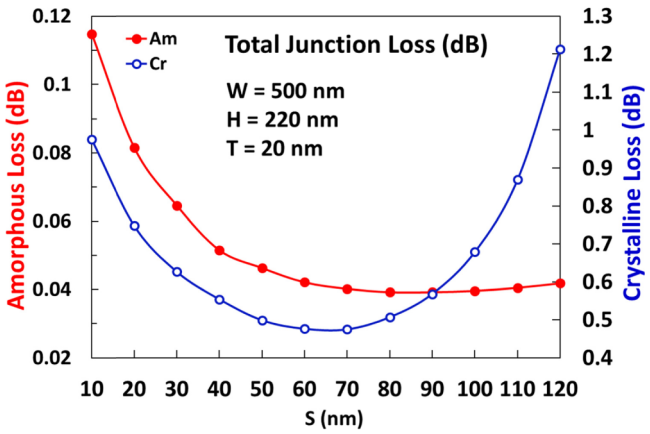

Fig. 13. Variation of the total junction loss of WG1 in amorphous and crystalline states with the slab thickness, S.

Next, effect of GST thickness T on the junction loss is studied. When the width is fixed at 500 nm and S = 90 nm for the amorphous state, the total junction losses from both the input and output junctions for WG1 as a function of GST thickness T are shown by a solid blue line in Fig. 14. For comparison, junction loss for GST clad nanowire waveguide WG2 at amorphous state is also shown by a dashed blue line. As T increases from 10 to 30 nm, the junction losses in both WG1 and WG2 increase and the WG2 always suffers from a higher loss value from 0.05 to 0.17 dB. For the crystalline state, the total junction losses in WG1, shown by a solid red line using the right-hand side scale, increase sharply from 0.1 dB to more than 3 dB. On the other hand, the total junction losses for WG2, shown by a dashed red line, increase monotonically from 0.33 to 1.66 dB. It can be concluded that when GST is in the crystalline state, the junction losses in WG1 will be unstable when T is more than 25 nm, but in WG2 the junction loss will be smaller. This study indicates that a thinner, 10-20 nm thickness GST layer would yield a lower junction loss value in both the states.

The associated insertion loss suggests that an optical switch at the ON state can be obtained when GST is in amorphous state. The total loss is comprised of the modal loss of the GST-Si hybrid waveguide section due to the absorption in the GST cap and the coupling loss between the passive input and output silicon waveguide sections and the active GST-Si hybrid waveguide section. Here, when W is fixed at 500 nm and T = 20 nm, the associated total insertion loss of WG1 is shown by a solid red line in Fig. 15. It can be observed that, when the slab thickness S increases from 10 to 120 nm, the total insertion loss of the switch reduces from 0.452 dB to a

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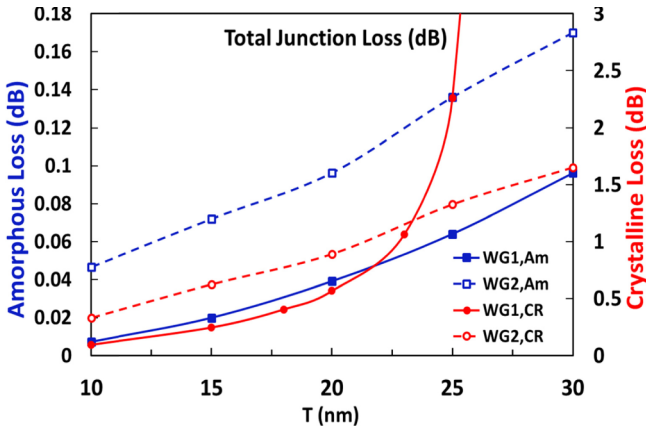

Fig. 14. Variation of the total junction loss of WG1 and WG2 in amorphous and crystalline states with the GST thicknesses, T.

relatively lower value of 0.352 dB, yielding a compact device with length smaller than 3.2 μm, as shown previously in Fig. 11.

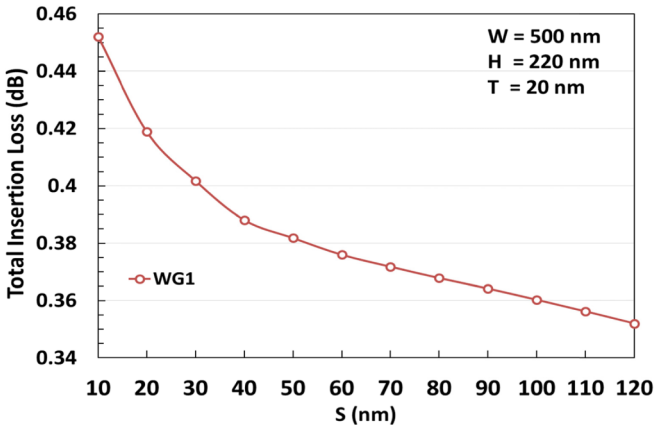

Fig. 15. Variations of total insertion loss of WG1 in amorphous state with slab thickness S.

Finally, variations of the total insertion loss with the GST thickness T for both the designs are shown in Fig. 16. Here, the width W is fixed at 500 nm and S = 90 nm (for WG1), the associated total insertion loss for the switch based on WG1 and WG2 is shown by the red and blue solid lines, respectively. It should be noted that for a thinner GST layer, although per unit distance modal loss (α_1) was lower, but the overall modal loss was higher, as an increased device length is needed to achieve the targeted 20 dB differential loss between the states. On the other hand, junction loss increases for a thicker GST layer, as the mode field profile deviates considerably from that of the input and output waveguides without a GST cover.

It can be observed from Fig. 16, that for the silicon rib waveguide WG1, the total insertion loss reduces from 0.4 dB to the minimum 0.36 dB as the T increases from 10 to 25 nm and then increases slightly to 0.367 dB at T = 30 nm. On the other hand, the total insertion loss for the silicon nanowire waveguide WG2 also decreases to a lowest value 0.433 dB as the T increases to 20 nm. After that, the insertion loss starts to increase slowly to a higher value with the thicker GST layer. It can be concluded that the silicon rib waveguide WG1 will have a smaller total

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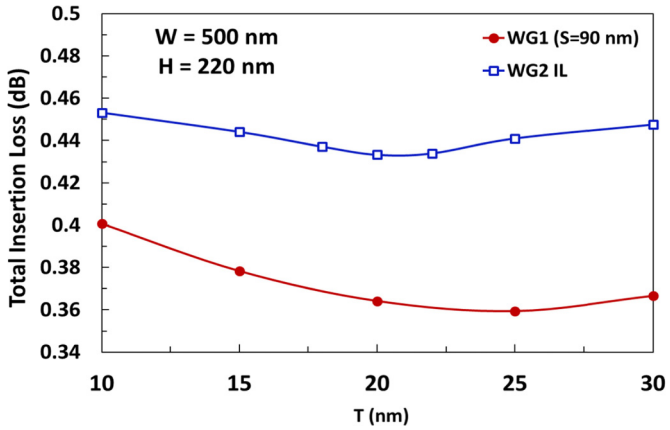

Fig. 16. Variations of the total insertion loss for WG1 and WG2 in amorphous state with the GST thickness, T.

insertion loss compared to the silicon nanowire waveguide WG2, and the minimum insertion loss can be achieved for a 25-nm-thick GST layer.

The switches have been designed to have modal loss in the crystalline state 20 dB higher than its amorphous state. However, as the junction loss for crystalline state is also higher than that of the amorphous state, so the total loss for the crystalline "OFF" state would be more than 20 dB higher than the low-loss amorphous "ON" state.

4. Conclusion

We have carried out rigorous modal analyses of a self-sustained switch based on a GST-clad silicon rib waveguide (WG1) and also a GST-clad silicon nanowire waveguide (WG2) for comparison at the telecommunication wavelength 1.55 μm by using an accurate **H**-field based FEM. We have also investigated the coupling loss at the butt-coupled junctions by using a rigorous junction analysis approach. It can be concluded that although GST cladding can yield a high ER values, however due to the associated higher EA values, a conventional MZI switch design will not be viable. On the other hand, design of EA-type switch would be preferred, which exploits the larger modal loss difference between the GST amorphous and crystalline states. Here, the effects of silicon slab thickness S, waveguide width W, and GST layer thickness T on device performances for both the WG1 and WG2 designs are presented.

It is shown here that the silicon slab height larger than 90 nm can yield a lower modal loss 0.34 dB at amorphous state but require a slightly longer device length around 3.1 μm. On the other hand, the slab thickness larger than 60 nm can yield a satisfactory design with a lower junction loss at amorphous state. This suggests that the slab thickness, S = 60-90 nm can be taken as an optimal design to balance the device length and also to achieve a lower insertion loss.

It can also be noted here, that a narrower silicon width W = 450 nm will not only yield a longer device length but also a larger modal loss. Therefore, a wider 500 nm silicon waveguide is preferred. It is also observed that, a thicker GST layer not only can reduce the total modal loss but also can yield a shorter device length. However, due to the mismatch of the modal fields, the junction loss would increase with the GST thickness. The optimal design needs to consider both these loss values. Here, we consider T = 15-25 nm as the optimal design as a thicker GST layer may produce unstable junction loss for the crystalline state. For comparison of the Si-GST rib waveguide WG1 with a fully etched Si-GST nanowire waveguide WG2, it is shown here, that the WG2 always suffers from a higher modal loss and a higher junction loss than that of WG1. It thus yields a higher total insertion loss, so the silicon rib waveguide WG1 is a preferred option

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for the optimal waveguide structure adopted for the switch. Additionally, WG1 rib waveguide maybe a preferred over fully-etched WG2 as WG1 will also have lower optical loss due to reduced scattering loss at the edges.

In summary, the GST-cladded silicon rib waveguide with a width W = 500 nm, a slab thickness S = 60-90 nm, and a GST thickness T = 15-25 nm can be considered as optimal design for the self-sustained switch. In this case, a very compact, 2-5 μm long device is expected to show an extinction ratio of more than 20 dB between the "OFF" and "ON" states with the total insertion loss of only 0.36 dB at the "ON" state.

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