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Analogue Hardware Based Algorithm
for Low-Power and Low-Voltage
Position Measurement Systems
with Enhanced Resolution

by
Karsten Leitis

Thesis Submitted for the Degree of

DOCTOR OF PHILOSOPHY

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Abstract

Position measurement systems are used in a wide variety of applications based on different sensing principles. Whatever the application or sensing method, they all share common issues of accuracy, robustness and power consumption. This thesis concentrates on two aspects of sensor interface design in order to achieve a very low power consumption for position measurement systems, in order to optimise their use for battery applications.

A new architecture and optimized components have been investigated with regard to low power and low voltage operation. The architecture establishes typical properties of position measurement systems such as linearization and resolution enhancement. A new method for resolution enhancement in respect of low power and low voltage system requirements is proposed within this work. The same major requirements are also fulfilled on a component level.

On an architectural level, the method utilizes signal symmetry provided by the sensor signal. A very common output signal of position measurement sensor elements establishes a sine and a cosine waveform. With folding and signal transformation techniques these signals are coarse converted and pre-processed before A/D conversion. As a result, the number of components is reduced and a significant amount of power is saved.

Many position measurement systems linearize the sensor element signals by digital computation. This work proposes a method of linearization within the A/D converter. The advantage is that no extra power consumption is involved because no additional elements are inserted into the A/D converter. By using a non-linear resistor network that composes the sine and cosine sensor signal, a linearized output is obtained. As a result the linearization algorithm is realised by an analogue hardware circuit. This has the added benefit of reducing the circuit noise, a common problem with digital circuits.

In addition to the architectural level design, new components realized as integrated circuit cells, contribute to a reduction of the overall power consumption. Both, the power supply voltage and the power supply current are significantly reduced. A trade-off between performance and reduction of

power consumption has been the basis of the circuit design. Circuit components that determine the minimum power supply voltage have been the subject of a thorough investigation in respect of sub-threshold or moderate inversion operation. As a result, a power supply voltage range smaller than given by the fundamental limits for strong inversion operation can be chosen. These components were realized as a physical cell design and implemented in the form of a test chip. Test results are reported that demonstrate the practical performance of the overall architecture and individual components.

A new error model has been developed for the overall sensor system in order to investigate the influence of parameter deviation and inherent errors. The model has been used in simulation studies that demonstrate the overall accuracy and robustness of the design.

The thesis concludes with a summary of the major achievements and an evaluation, in the form of a comparison with existing systems.

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List of Symbols

Symbol	Description	Unit
α	transistor dimension ratio for hysteresis voltage	1
α_{R0}	temperature coefficient of R_0	K
$\alpha_{\Delta R}$	temperature coefficient of the hub of the resistance	K
α_{off}	power supply dependent temperature coefficient of the offset	K
β	transconductance coefficient	A/V^2
β_f	feedback factor	1
γ	body effect parameter	\sqrt{V}
λ	channel length modulation	$1/V$
μ	charge carrier mobility	cm^2/Vs
ω_t	unity gain frequency	$1/s$
ϕ_F	Fermi potential	V
φ	phase angle of the sensor element signals	rad
φ_k	ideal discrete phase angle	rad
ψ_{min}	minimum resolution	m
d_{off}	power supply dependent offset	A / V
g_m	transconductance	A / V
g_d	drain conductance	A / V
g_{mw}	transconductance weak inversion	A / V
g_{mm}	transconductance moderate inversion	A / V
g_{dw}	drain conductance weak inversion	A / V
g_{dm}	drain conductance moderate inversion	A / V
i_{dwn}	white noise drain current	A
$i_{dwn,w}$	white noise drain current in weak inversion	A
n	weak inversion slope factor	1
q	electron charge	C
r_{off}	offset equivalent resistance	Ω
u	inversion coefficient	1
v_n	noise voltage	V
v_{dwn}	white noise gate voltage	V
$v_{dwn,w}$	white noise gate voltage in weak inversion	V
v_{fn}	flicker noise voltage	V
A_0	open loop amplification	dB
A_c	amplitude of the cosine	V
A_f	differential voltage amplification with feedback	dB
A_s	amplitude of the sine	V
A_v	differential voltage amplification	dB
B_2	Early voltage parameter	$V \cdot \sqrt{cm}$

List of Symbols

Symbol	Description	Unit
C'_{ox}	gate oxide capacitance	F/m^2
C_{ox}	normalized oxide capacitance	F/m^2
DNL	differential nonlinearity	1
DR	dynamic range	dB
H_0	intrinsic characteristic magnetic field	A/m
H_x	extrinsic magnetic field in x-direction	A/m
H_y	extrinsic magnetic field in y-direction	A/m
INL	integral nonlinearity	1
I_{bias}	bias current	A
I_d	drain current	A
I_{ds}	drain-source current	A
I_S	specific current, upper limit in weak inversion	A
I_Z	geometry dependent specific current	A
L	channel length	m
N_A	acceptor concentration	m
P	period	m, t, rad, °
P_t	position corresponding voltage	m, t, rad, °
Q	minimum sensor resolution	m
ΔR	maximum change of the magneto resistance	Ω
R_0	magneto resistance without magnetic field	Ω
R_{25°	magneto resistance at room temperature	Ω
R_{tot}	total resistance of the resistor chain	Ω
SNR	signal to noise ratio	dB
S_r	slew rate	V/s
V_A	Early voltage	V
V_{bs}	bulk-source voltage	V
V_{ds}	drain-source voltage	V
V_{dsat}	drain-source saturation voltage	V
V_{eff}	effective gate-source voltage	V
V_{gs}	gate-source voltage	V
$V_{gs,n}$	gate-source voltage n-channel transistor	V
$V_{gs,p}$	gate-source voltage p-channel transistor	V
V_{hys}	hysteresis voltage	V
$V_{in,cm}$	common mode input voltage	V
V_n	rms noise voltage	V
V_{ref}	reference voltage	V
V_{th}	threshold voltage	V
V_{off}	offset voltage	V

List of Symbols

Symbol	Description	Unit
V_x	tap voltage of resistor ladder	V
V_{x_i}	discrete tap voltage of resistor ladder	V
V_{ACs}	voltage amplitude of the sensor	V
V_{DCs}	dc voltage level of the sensor	V
V_{DD}	power supply voltage	V
$V_{DD,min}$	minimum power supply voltage	V
V_{SS}	negative power supply voltage	V
V_T	thermal voltage	V
W	channel width	m

List of constants

Symbol	Description	Value	Unit
ϵ_{ox}	permittivity of silicon dioxide	$3.45 \cdot 10^{-13}$	F/cm
ϵ_{si}	permittivity of silicon	$1.04 \cdot 10^{-12}$	F/cm
k	Boltzmann Constant	$1.387 \cdot 10^{-23}$	$\frac{V \cdot C}{K}$
q	magnitude of electron charge	$1.602 \cdot 10^{-19}$	C
μ_{m0}	magnetic field constant	$1.256637 \cdot 10^{-6}$	$\frac{V \cdot s}{A \cdot m}$

Chapter 1

Introduction

1.1 Overall Sensor System

In many of today's appliances and applications it is useful or necessary to determine the positions like length and angle, for instance in brake systems of a car or in industrial sawing machines. Hence a market has grown with a broad variety of functionality and features. Some things have become established such as interfaces at the input and output, methods for resolution enhancement or typical supply voltages.

Various types of physical effects are used for position measurement like optical, capacitive, inductive or magnetic sensor phenomena. Magneto resistive sensors are based on the anisotropic magneto resistive effect and are well suited for this measurement task, because they are able to work in harsh environments compared with other sensor principles like optical [1] or capacitive position sensors. One further advantage is that they can be produced as integrated devices with lithographic processes in very high volumes at low chip prices.

Anisotropic Magneto Resistive (AMR) sensor elements exhibit changes of resistance within external moving magnetic fields. The phenomenon effect is a change of the conductivity of the material (Permalloy) as a function of an extrinsic magnetic field. Typically, the resistors are arranged in Wheatstone bridges, in order to provide differential signals with common mode rejection. At the output they provide a signal, which is comparable to other measurement systems for instance laser tracking systems [2] or optical encoders which generate quadrature sinusoidal signals by optical slits [3]. Some of these sensors generate two sine waveforms which normally show a phase shift of 90° . Based on these two signals, different signal processing methods have been developed.

Essentially two properties of these signals are used. First, the phase shift between both signals indicates a direction, because the shift can be either plus or minus 90° . Second, some mathematical procedures have been established for linearization and interpolation [4]. Those algorithms can be implemented in software, based in arithmetic logic units, or hardware based in digital or analogue signal processing units. With these methods the resolution of such measurement systems can be increased.

This work contributes to an advance in position measurement systems. It focuses on one main topic: "Reduction of the total power consumption"

All of the known systems work within a conventional supply voltage range of 3 V to 5 V, but they are not optimised with respect to the power consumption. In order to minimise power consumption the supply voltage has to drop. This is also a requirement for future technologies for integrated circuits. Due to reliability aspects, the supply voltage has also to be reduced for newer technologies with reduced geometries of electronic elements [5]. Wake up systems or non-continuous time systems can be used to reduce consumption but they do not solve the basic problem that the supply voltage must drop. The focus of this work is an optimised signal processing circuit that operates at a minimised supply voltage. Basically the circuit should be driven at the lowest possible voltage supplies while maintaining an appropriate level of performance. Fundamental margins are given for the minimum voltages to drive MOS transistors and CMOS circuits.

1.2 Sensor

Magneto resistive sensors are also able to work at low voltages. The minimum possible supply voltage is limited by the signal to noise ratio [6]. By reducing the supply voltage the power consumption of the sensor also decreases. Therefore the magneto resistive sensor is well suited for position measurement at low-voltages and low-power due to available high impedance sensor bridges. This type of sensor does not limit the system requirements. All borders are given by the electronics and require new architectures to find the margins of operation.

1.3 Electronics

In order to reach the aim of the thesis the problem was divided into two parts. First, the component level influences significantly the power consumption.

Second, special architectures at system level can contribute to an advance in saving power consumption.

The purpose on component level is to develop basic cells for integrated circuits. Necessarily, special integrated circuit components have to be developed because such components as needed are not available for this sensor application. Researchers invested considerable effort to develop low-voltage analogue cells in order to facilitate the decrease of the power supply voltages down to usual power supply voltages for digital circuits. On the one hand, layouts and element dimensions of these developed analogue cells are not compatible for different processes but on the other hand methods and topologies can be transferred to other technologies. Due to that a lot of solutions for low-voltage and low-power operation are valid for other CMOS technologies.

At the element or transistor level, the lowest operating voltages and lowest operating currents are reached, if the transistor is driven in the weak inversion or sub-threshold region. Circuit developments based on this operating region of transistors allow operating voltages down to the lowest fundamental limits. Traditionally, circuit designers set the margins for the transistor operating region to the lowest possible value in the strong inversion region.

One major shortcoming occurs by driving the transistor in the sub-threshold region, where the MOS transistors behave similarly to bipolar transistors. This insufficiency is serious. Due to the drastic current reduction the frequency bandwidth is significantly decreased. Nevertheless components such as OPAMPs must be developed which are sufficient for the frequency requirements of the system. If, for instance, the position measurement system needs a 3dB frequency of about 10 kHz and a gain of 30, then a gain bandwidth product of 300 kHz would be sufficient. This is a typical value for many applications. Hence application specific developments with reduced power supply voltages and bias currents must advance this position measurement system.

Some techniques are proposed to enhance gain and bandwidth in weak inversion operation up to 5 times [7]. But in order to save as much power consumption as possible the circuit topologies should be kept as simple as possible. Any additional circuit element needs to be driven and consumes power. An improvement in gain and bandwidth is only advisable if it is required.

Basically, analogue circuits operate with operational amplifiers and comparators. Therefore the focus is set on these components. The dynamic range for such components is reduced if the power supply voltage decreases. Hence, it becomes more important to get rid of limitations that are governed by the component architecture. For instance, the differential amplifier should

have a rail-to-rail input and output characteristic. This influences also the smallest possible supply voltage. The problem is to find architectures that enlarge the power supply voltage requirement by only a small amount.

One further problem refers to the threshold voltage. In contrast to the reduction of the power supply voltages for newer technologies, the threshold voltage decreases only slightly [5]. As a result, the ratio of the supply voltage to the threshold voltage decreases and analogue signal processing suffers due to the loss of headroom. This means that the threshold voltage determines significantly the minimum possible power supply voltage.

1.4 Linearization and Interpolation

On the system level, two fundamental requirements exist. First, at the input, nonlinear signals drive the electronic circuit, whereas at the output linear signals are expected. The circuit has therefore to provide a method of linearization. Second, the resolution of the position sensor must be improved by electronic signal processing in order to bypass the limited resolution that is given by the sensing element.

Existing methods linearize the signal with digital [2], [3], [8], [9] as well as analogue techniques [10, 11] but these methods are neither developed for low voltage operation nor optimised accordingly for low power consumption and are not suitable for battery applications with long battery lifetime.

Furthermore, digital linearized and interpolated signals consume substantial power if they work with a high clock frequency. This means considerable power consumption. Hence the digital computation must be reduced or prevented. An important issue here is how many digital computations are necessary? Could the same task be done by an analogue circuit with less power consumption?

Methods that linearize and interpolate the signal in an analogue way, use a large number of components like OPAMPs and comparators. For instance, if an ADC with a flash topology is to be operated over the complete supply voltage range, then a lot of comparators are required for high resolutions and the analogue input signal should have large amplitudes in order to minimise the quantization error. Therefore, an amplitude independent method is needed as proposed by [12]. This method suffers, however, from high power consumption, as a large number of redundant components is required in order to convert an analogue input signal that provides an intrinsic symmetry.

A further objective of this thesis is, therefore, to find an improved topology that reduces the power consumption and also works at the minimum limits of the supply voltage range.

Two very important requirements for position measurement systems are the position resolution and the accuracy. The accuracy of a sensor system is not entirely predictable, because offset, mismatch and parameter scatter of elements and components cannot be easily determined, but the accuracy can be estimated by worst case assumptions of components. That means also the accuracy is strongly influenced by the topology and layout of the components. One task is therefore to develop layouts which minimise the accuracy problem and give careful consideration of the component arrangement, which influence the accuracy. For example, resistors must be matched, the higher the number of resistors that are related together the higher the overall error. The dimensions of the resistors must be a compromise of accuracy and chip area. An error model which takes all errors into account must be developed to estimate the overall error and to determine the main influences. Furthermore, with such a model the influence of the matching is valuable.

Concerning the resolution, the position sensing system should have a resolution that is much higher than the resolution that is given by the sensor. There is a direct relationship between the resolution and the quantization of the A/D Converter. Hence, a topology must be found that operates on the one hand at low supply voltages and that saves energy by saving components and on the other hand allows a high resolution by maintaining or improving the dynamic range. The method should take into consideration that the achievable resolution is in correlation to the required precision. A scalable resolution would deal with either high resolution with less accuracy or with low resolution with an advanced accuracy. One key task is to find and evaluate a topology for resolution enhancement.

1.5 Conceptual Formulation and Purpose

This work covers four main topics.

First, the development of basic analogue cells which is presented in chapter 2. These cells are the fundamental integrated circuit cells that are used for the work on the system level.

Second, the system level is presented in chapter 3 and includes a special methodology for signal conditioning, particularly a new A/D conversion concept and signal linearization, respectively.

Third, models for the sensor and the system architecture are presented in chapter 4. This includes investigations on the system accuracy.

Fourth, in chapter 5 the measurement and simulation results are presented. This chapter ends with a discussion of the simulation and measurement results.

Chapter 2

Low-Power and Low-Voltage Integrated Circuit Cells

2.1 Fundamental Limitations

2.1.1 Large Signal MOSFET Model

Strong Inversion

The operating range of MOS transistors can be separated into two regions [16], the triode (or linear) and the saturation (or active) region, each of which is described by special model equations. Within the so-called triode region the transistor is not saturated and the drain current I_d can be written by the following expression 2.1.

$$I_d = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[(V_{gs} - V_{th}) \cdot V_{ds} - \frac{1}{2} V_{ds}^2 \right] \quad (2.1)$$

$$\text{for } V_{gs} \geq V_{th} \text{ and } V_{ds} < V_{dsat} = V_{gs} - V_{th} = V_{eff} \quad (2.2)$$

Equation 2.1 contains the fixed parameters channel width W , channel length L , the oxide capacitance per unit area C_{ox} and the technology dependent mobility μ (for NMOS μ_n , for PMOS μ_p). In this domain, the transistor is driven with the gate-source voltage V_{gs} and the drain-source voltage V_{ds} . The threshold voltage V_{th} can generally be assumed to be constant, particularly if no body effect occurs.

If V_{ds} leaves the range of definition 2.2, the transistor is saturated. In this range the drain current is specified by equation 2.3.

$$I_d = \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{gs} - V_{th})^2 (1 + \lambda \cdot V_{ds}) \quad (2.3)$$

$$\text{for } V_{gs} \geq V_{th} \text{ and } V_{ds} \geq V_{dsat} = V_{gs} - V_{th} = V_{eff} \quad (2.4)$$

The channel length modulation λ in equation 2.3 is often small and may be ignored. Hence, $\lambda \cdot V_{ds} = 0$ is assumed and equation 2.3 becomes independent of the drain-source voltage.

In low-voltage and low-power circuit design the meaning of strong inversion operation of MOS devices is high. Such circuits operate at the margins of the operating range, which are determined by the definition 2.4, by maintaining the typical performance of integrated circuits that typically operate at higher power supply voltages and bias currents. From the performance viewpoint, like signal processing speed and noise considerations, strong inversion operation is the best choice.

In contrast, the strong inversion operation is not preferred if system requirements enforce lower power supply voltages and lower power consumption. In this case the devices can be driven below the threshold of the devices.

Weak Inversion

From the definition 2.2 and 2.4 it is given that when $V_{gs} \geq V_{th}$ the transistor is driven in the strong inversion region. This is the classical operation region for circuit development. If $V_{gs} < V_{th}$ then the operation region changes into the weak inversion (or subthreshold) region and the drain current becomes very small. Circuit developments with radically reduced current consumption work with very small currents below the threshold voltage e.g. battery supply applications. The behaviour of MOSFETs driven in this operating domain is similar to a bipolar transistor. Expression 2.5 describes the drain current in the subthreshold operating domain - the weak inversion domain - of MOS transistors.

$$I_d = I_S \cdot \frac{W}{L} \cdot e^{\frac{V_{gs}-V_{th}}{n \cdot V_T}} \cdot \left(1 - e^{-\frac{V_{ds}}{V_T}}\right) \cdot e^{-V_{bs} \cdot \left(\frac{1}{n \cdot V_T} - \frac{1}{V_T}\right)} \quad (2.5)$$

In equation 2.5 the thermal voltage V_T is calculated by $V_T = \frac{k \cdot T}{q}$ with Boltzmann's constant $k = 1.387e - 23 \text{ VC}/^\circ\text{K}$, the electronic charge $q = 1.6e - 19 \text{ C}$ and the temperature T . At room temperature $V_T \cong 26 \text{ mV}$. Depending on the technology the slope factor n is typically in the range of 1 to 2. Also the *specific current* I_S is a technology constant and describes the current performance of the current in the weak inversion domain. I_S is calculated as follows (Eq. 2.6):

$$I_S = 2 \cdot n \cdot \mu \cdot C_{ox} \cdot V_T^2 \quad (2.6)$$

It is almost always valid to neglect the influences of V_{ds} and V_{bs} in equation 2.5 for hand calculation. V_{bs} is set to zero, if the body effect can be prevented and if $V_{ds} > 4 \cdot V_T$ then the drain-source voltage is also negligible. The influence of V_{ds} is then smaller than 2%. Equation 2.5 can then be simplified as expressed in equation 2.7.

$$I_d = I_s \cdot \frac{W}{L} \cdot e^{\frac{V_{gs} - V_{th}}{n \cdot V_T}} = I_Z \cdot e^{\frac{V_{gs} - V_{th}}{n \cdot V_T}} \quad (2.7)$$

$$\text{for } V_{ds} > 4 \cdot V_T \quad (2.8)$$

The transistor model of equation 2.7 is assumed to be saturated due to the fact that the drain current is independent of the drain source voltage. Therefore the saturation condition 2.8 must be fulfilled. Sometimes designers set the saturation margin to $6 \cdot V_T$ or higher in order to reach more robustness and reliability. For evaluation of minimum supply voltages the margin is taken at the lowest value of condition 2.8.

Weak inversion operation of MOS devices has become popular since low-power and low-voltage applications are required. Often only parts of a circuit are biased with very low currents and below the threshold of the devices. The correlation between I_d and V_{gs} can be used to lower V_{gs} in order to reduce the power supply voltage range which is mainly determined by V_{gs} . For low-voltage design low technology dependent V_{th} of n-channel and p-channel devices are desired.

But due to the resulting low currents in weak inversion operation the signal processing speed is drastically decreased and also the noise level rises (sec. 2.1.6). A trade-off between strong and weak inversion operation might be the moderate inversion region.

Moderate Inversion

The transition between the strong and the weak inversion operation of a transistor is smooth and the so-called moderate inversion region. This region is defined by (Eq. 2.9):

$$\frac{1}{10} I_d < I_Z < 10 I_d \quad (2.9)$$

No explicit model is available for only this intermediate region. As reported in [17] many problems can occur in simulation regarding the simulation accuracy. Several semi empirical expressions have been developed, for example [18]. Another approach is proposed in [19] which is dedicated to the design and analysis of low-voltage and low-current analogue circuits.

With this model a balanced compromise between accuracy and simplicity is achieved. This model covers all regions of operation from strong inversion to weak inversion inclusive of moderate inversion and in addition saturation and non-saturation. This model is normally known as the bulk referred model [17], but if it is extended a source referenced model can be written as

$$I_{ds} = 2n\mu C_{ox} V_T^2 \frac{W}{L} \left\{ \left[\ln^2 \left(1 + e^{\frac{V_{gs} - V_{th}}{2nV_T}} \right) \right] - \left[\ln^2 \left(1 + e^{\frac{V_{gs} - V_{th} - nV_{ds}}{2nV_T}} \right) \right] \right\} \quad (2.10)$$

Equation 2.10 can be simplified for transistors in saturation. Then the second term becomes negligible. Thus the equation can be expressed by

$$I_{ds} = 2n\mu C_{ox} V_T^2 \frac{W}{L} \left[\ln^2 \left(1 + e^{\frac{V_{gs} - V_{th}}{2nV_T}} \right) \right] = I_Z \left[\ln^2 \left(1 + e^{\frac{V_{gs} - V_{th}}{2nV_T}} \right) \right] \quad (2.11)$$

The model equation 2.11 is valid in all regions of inversion if the transistor is saturated. The slope factor n is given by

$$n = 1 + \frac{\gamma}{2\sqrt{V_{sb} + \phi_F}} \quad (2.12)$$

where V_{sb} is the source-bulk voltage. ϕ_F , the Fermi potential, can be written as

$$|\phi_F| \approx \left| V_T \ln \frac{N_A}{n_i} \right| \quad (2.13)$$

with N_A the acceptor concentration and n_i the intrinsic carrier concentration. Depending on the doping concentration the Fermi potential is at room temperature between 0.23 and 0.47. A good approximation is therefore 0.35.

The parameter γ in equation 2.12 for the slope factor is as follows:

$$\gamma \equiv \frac{\sqrt{2q\epsilon_{si}N_A}}{C_{ox}} \quad (2.14)$$

where q is the electron charge, ϵ_{si} is the permittivity of silicon, N_A the acceptor concentration and C_{ox} the gate capacitance per unit area. Typical values for γ are in a range of 0.2 and 2.0. If for example $\gamma=0.8$ and $\phi_F=0.35$ and no body effect is present and therefore $V_{sb}=0$, the slope factor n is ≈ 1.7 , which can be taken for rough estimations.

Regarding the performance, moderate inversion operation is a good compromise if power consumption and the power supply voltage should be reduced. The model behaviour around the threshold voltage of the device is less accurate than other models in respect of hand calculations. Nonetheless

this large signal model provides the opportunity for circuit calculations for devices that are neither operated in strong nor in weak inversion. The meaning of driving circuits or parts of a circuit in moderate inversion has become more usual. Also in this work the moderate inversion region is often used for circuit parts.

The large signal models are used for determination of drain current as well as for calculations of V_{gs} . Particularly the determination of V_{gs} is important in order to define the mode of operation.

2.1.2 Small Signal MOSFET Model

Strong Inversion

When using the small signal analysis model of MOSFET transistors, it is important to take the operating point into account. This was briefly discussed in chapter 2.1.1, where the operating point is adjusted with the drain current. The derivation of equation 2.3 with respect to the gate-source voltage gives the transistor transconductance g_m as expressed in equation 2.15.

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \sqrt{2\beta I_d} \quad (2.15)$$

If equation 2.3 is derived with respect to the output or drain-source voltage, then the result is the output conductance of the transistor (Eq. 2.16).

$$g_d = \frac{\partial I_d}{\partial V_{ds}} \approx \lambda \cdot I_d \quad (2.16)$$

Weak Inversion

For the weak inversion region, the model for the drain current is given by equation 2.5. As discussed above, the derivations with respect to the gate-source voltage and the drain-source voltage give the small signal parameters (Eq. 2.17, 2.18).

$$g_{mw} = \frac{\partial I_{dw}}{\partial V_{gs}} = \frac{I_d}{n \cdot V_T} \quad (2.17)$$

$$g_{dw} = \frac{\partial I_{dw}}{\partial V_{ds}} = \frac{1}{e^{\frac{V_{ds}}{V_T}} - 1} \cdot \frac{I_d}{V_T} \quad (2.18)$$

The derivation of the drain current with respect to the drain source voltage is beset with a problem. If V_{ds} becomes very large, which indeed is

a typical case, then g_{dw} converges against zero or r_{dw} becomes infinite, respectively. This is very inaccurate and not useful. The model for g_d is better expressed by the equation 2.23 from the all region model which is particularly true for moderate inversion.

Conspicuous in both equations 2.17 and 2.18 is that both the transconductance g_{mw} and the output conductance g_{dw} depend on V_T and hence on the temperature. This implies for the circuit development, that only in the case of relations where V_T is cut a compensation of the temperature is partially or completely possible. This particularly influences the poles and zeros of the frequency response. As a consequence the 3dB frequency is shifted over temperature and makes the compensation of amplifiers difficult.

Moderate Inversion

The small signal model in moderate inversion is similar to the weak inversion model. The calculation is based on the inversion coefficient u which is defined by

$$u = \frac{I_d}{I_Z} \quad (2.19)$$

With equation 2.19 a special function can be expressed which is used in several further equations.

$$f(u) = \frac{1}{2}(\sqrt{1 + 4u} + 1) \quad (2.20)$$

This equation is used in the expression for the transconductance which is given by

$$g_{mm} = \frac{I_d}{nV_T} \frac{1}{f(u)} \quad (2.21)$$

The conductance for transistors in moderate inversion is based on the Early voltage as for bipolar transistors. The Early voltage is given by

$$V_A = B_2 \cdot L \cdot \sqrt{N_A} \quad (2.22)$$

where N_A is the acceptor concentration, L is the gate length and B_2 is a parameter which is in a range of $1 \cdot 10^{-3}$ to $2 \cdot 10^{-3} V \cdot \sqrt{cm}$. In conjunction with equation 2.22 the conductance is

$$g_{dm} = \frac{I_d}{V_A} \quad (2.23)$$

The transconductance is employed in several equations for circuit calculation. The right small signal model should be applied for hand calculation in order to achieve the highest accuracy compared with the simulation and measurement results.

2.1.3 Minimum Supply Voltage Range

Analogue circuits which operate with significantly reduced supply voltages may work at the fundamental margins of the elements. As described in chapter 2.1.1 one of the limiting parameters for saturated transistors is the minimum drain-source V_{ds} voltage. The voltage must be larger than $4V_T \approx 100mV$. This is much less than for transistors working in the strong inversion domain. For calculations of the minimum supply voltage margins of CMOS circuits, the number of stacked transistors between the supply voltages is vital. The smaller the number of transistors the smaller the minimum supply voltage may shrink. But it is not only V_{ds} that determines the supply voltage range. V_{gs} has the most important significance for the calculation of the minimum possible supply voltage. Both, V_{gs} and V_{ds} determine the minimum power supply voltage, which can be expressed for a single simple gain stage by equation 2.24.

$$V_{DD,min} = V_{gs} + V_{ds} = V_{th} + V_{eff} + 4V_T \quad (2.24)$$

For circuit developments using the strong inversion region V_{gs} is larger than V_{th} . If the circuit is driven in the weak inversion region V_{gs} can be chosen smaller (below V_{th}). Therefore, with respect to the minimum possible power supply it is an advantage to drive analogue circuits in the weak inversion region. The minimum possible power supply voltage can only be achieved for very simple topologies like single stage amplifiers, because only one gate-source voltage and one drain-source voltage limit the number of components. For example, if the threshold voltage is 0.6 V the minimum resulting strong inversion supply voltage is $V_{DD,min,si} = V_{gs} + V_{ds} = 0.6V + 0.2V + 0.4V = 1.2V$ and for weak inversion $V_{DD,min,wi} = V_{gs} + V_{ds} = 0.6V - 0.1V + 0.1V = 0.6V$. For more complex circuits, the minimum power supply voltage increases mostly by some further stacked saturation voltages. As a result the circuit topology should have less stacked or cascoded elements but more cascaded elements. In the following chapters it is described that most analogue circuits, such as OPAMPs, need higher supply voltages due to their more complex architectures.

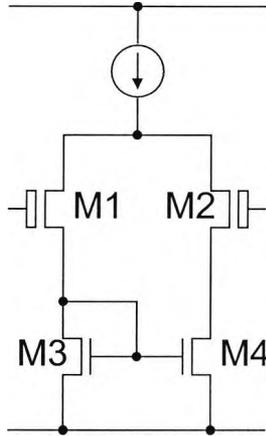


Figure 2.1: Simple differential amplifier with an active current mirror load

2.1.4 Differential Input Stages

Conventional differential input stages consist of a differential input transistor pair, a current source and a load, which is usually an active transistor in CMOS circuits. Depending on the type of input transistor pair, PMOS or NMOS, the common mode input range is limited to either the positive or to the negative power supply voltage range. Differential input stages which work with an active current mirror load are limited in respect of the common mode input range [31],[32].

Figure 2.1 shows an input stage of a conventional differential amplifier with an active current mirror load. In contrast to a resistive load, the voltage drop for an active load is at a minimum one gate-source voltage. This is caused by the diode-connected-transistor M3. The common mode input range is reduced, due to the shift of the drain potential to one gate-source voltage [33]. The common mode input range is therefore given by (Eq. 2.25)

$$V_{ss} + V_{gs,n} + V_{th,p} \leq V_{in,cm} \leq V_{DD} - V_{ds} - V_{sg,p} \quad (2.25)$$

where $V_{gs,n}$ represents the gate-source voltage of the load transistor, $V_{th,p}$ the threshold voltage of the PMOS input transistors, V_{ds} the drain-source voltage of the current source and $V_{sg,p}$ the gate-source voltage of the input pair. M3 may push the drain potential of M1 out of saturation at low power supply voltages.

As a result, this problem must be avoided for low voltage operations. Instead of diode-connected-transistors, load transistors which operate with only one saturation voltage should be used. Such topologies have a signifi-

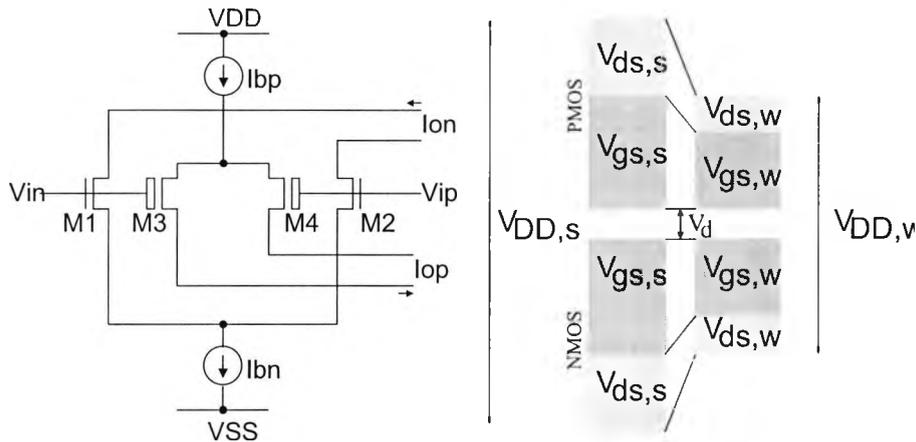


Figure 2.3: Rail-to-rail input stage

differential pair close to V_{DD}) with a very small headroom, the power supply voltage can be as small as possible without the property of a signal processing reaching from the negative to the positive supply voltage at the input.

In order to overcome this limit a PMOS and a NMOS differential input stage must be put in parallel. Then the signal processing is possible over the complete common mode input voltage range reaching from the negative to the positive supply rail. Figure 2.3 shows this architecture.

Concerning the requirement of a minimum power supply, rail-to-rail input stages need the double supply voltage compared with a single one. This is indeed a drawback, but in most applications of OPAMPs in low-voltage environments rail-to-rail input stages are necessary due to the fact that the operation points at the amplifier input are mostly at $V_{DD}/2$. This is not feasible with single input stages that operate at their minimum possible power supply voltage.

The minimum power supply voltage for a rail-to-rail input stage is given by

$$V_{DD,min} = 2V_{gs} + 2V_{ds} \quad (2.27)$$

if $V_{gs,n} = V_{gs,p}$ and $V_{ds,n} = V_{ds,p}$. Equation 2.27 is valid for all operation regimes. In order to satisfy these conditions the current sources have to conduct the same current. In addition, the unequal charge carrier mobilities of PMOS and NMOS transistors $\mu_{0,p}$ and $\mu_{0,n}$ should be equalized by the W/L ratios. In order to balance out the drain-source voltages of the current sources, the different charge carrier mobilities should be compensated and the gate-source voltages should be the equal.

Figure 2.3 shows all voltages which determine the minimum power supply voltage. The minimum is reached if v_d is ≈ 0 . In traditional circuit design v_d is in a range of some volts. Each of the traditional circuits would also allow the power supply to be reduced down to $v_d \approx 0$. The smaller V_{th} the smaller V_{DD} can be. If the input stage is biased in the weak inversion domain the power supply voltage is further reducible because V_{gs} and V_{ds} shrink compared with a signal processing biased in the strong inversion region. This is indicated by the suffixes „s” and „w” of the voltages.

One drawback regarding the power consumption is that such input stages consume a double current because both input stages need to be biased separately. Moreover, the additional transistors enlarge the dimensions of the layout and the used chip area.

2.1.6 Component Noise

MOS transistors have so far been assumed to be only time dependend on terminal voltages, but this not exactly true. The following considerations refer to an inherent noise of MOS transistors and not to interference noise of the system or the environment. The sensor element correlated noise which occurs in addition is discussed in section 3.1.2. Inherent noise is a fundamental circuit property and cannot be eliminated but may be reduced if the resulting equations of this chapter are taken as design rules. The drain current exhibits current fluctuations - the so-called random noise - which can be an important item in circuit design even if the signal to noise ratio is reduced by smaller supply voltages that limit the signal magnitude. The signal-to-noise ratio SNR of a signal node in a circuit is defined as

$$SNR \equiv 10 \log \left[\frac{\text{signalpower}}{\text{noisepower}} \right] \quad (2.28)$$

In the time domain the noise voltage $v_n(t)$ is defined by its rms value as

$$V_n \equiv \sqrt{\frac{1}{T} \int_0^T v_n^2(t) dt} \quad (2.29)$$

If one or more further noise sources exist, they have to be added as voltage or current sources based on Kirchhoff's law. For two individual voltage noise sources the total voltage noise is given by

$$v_{n,tot}(t) = v_{n1}(t) + v_{n2}(t) \quad (2.30)$$

Equation 2.30 becomes particularly important with regard to the total noise at the interface between the sensor element and the electronic circuit,

where the noise sources have to be added. At the drain of a DC biased single MOS transistor the current can be expressed as

$$i_{ds}(t) = I_d + i_n(t) \quad (2.31)$$

where I_d represents the DC current and $i_n(t)$ the noise current of the transistor. Two dominant noise sources exist in MOS transistors. One is called flicker noise and the other white noise.

White Noise in the Strong Inversion Region

The transistor channel between the source and the drain has a resistive property. As is known in simple resistors there is a noise component which depends on the resistance itself and the temperature. The same phenomena occurs in the channel of the transistor which can be derived from the white¹ noise from a resistor. In the triode region the resistance is the drain-source resistance of the transistor. If the transistor is in the active region the resistance is not homogeneous and therefore the resistance has to be integrated over the channel [16]. The resistance can be approximated as $R \approx 3/2g_m$. For simplification the noise is considered at $V_{ds} = V_{gs} - V_{th}$ as

$$\overline{i_{dwn}^2} = 4kT \frac{2}{3} g_m \cdot \Delta f \quad (2.32)$$

$$= 4kT \left[\frac{2}{3} \frac{W}{L} \mu C_{ox} (V_{gs} - V_{th}) \right] \cdot \Delta f \quad (2.33)$$

The white noise drain current i_{dwn} in equation 2.33 depends on Boltzmann's constant k , the temperature T and the transconductance g_m . If g_m is substituted, the noise current can be expressed depending of V_{gs} .

Sometimes it is useful to transform the noise current into an equivalent input noise voltage². Then the white voltage noise v_{gwn} is *gate-referred* given by

$$\overline{v_{gwn}^2} = 4kT \left(\frac{2}{3} \right) \cdot \frac{1}{g_m} \cdot \Delta f \quad (2.34)$$

Both i_{dwn} and v_{gwn} depend naturally on the temperature, but also on bias conditions and the element dimensions because of the transconductance g_m , which is given by equation 2.15.

¹White noise is often called thermal noise because the spectral density function depends on the temperature $v_n^2(f) = 4kTR$, where k is Boltzmann's constant, T the temperature and R the resistance

²In the small signal model the drain current can be expressed as $I_d = V_{gs} \cdot g_m$

White Noise in the Weak Inversion Region

White noise in the weak inversion region is not identical compared with the white noise in the strong inversion region [34]. Devices operating in saturation, which is achieved if $V_{ds} \geq 4$ to $6 V_T$, have a noise current of

$$\overline{i_{dwn,w}^2} = 2qI'_{ds}(1 + e^{-\frac{V_{ds}}{V_T}}) \cdot \Delta f \quad (2.35)$$

where q is the electron charge and I'_{ds} the drain current in the saturation.

One result of equation 2.35 is that the term $1 + e^{-\frac{V_{ds}}{V_T}}$ is negligible in saturation because at the minimum of $4V_T$ the influence of V_{ds} is only 2 percent.

In order to obtain a similar result to the strong inversion region, equation 2.35 can be expressed in terms of g_{mw} . Substituting I'_{ds} by equation 2.17 and the thermal voltage V_T by $V_T = kT/q$ gives

$$\overline{i_{dwn,w}^2} = 2nkT \cdot \left(1 + e^{-\frac{V_{ds}}{V_T}}\right) \cdot g_{mw} \cdot \Delta f \quad (2.36)$$

$$= 2q \cdot I_s \cdot \frac{W}{L} \cdot e^{\frac{V_{gs} - V_{th}}{nV_T}} \cdot \left(1 + e^{-\frac{V_{ds}}{V_T}}\right) \cdot \Delta f \quad (2.37)$$

The equivalent input noise voltage of equation 2.37 can be derived if $I_d = g_{mw} \cdot v_{gs}$ is applied. This results in

$$\overline{v_{gwn,w}^2} = 2nkT \cdot \left(1 + e^{-\frac{V_{ds}}{V_T}}\right) \cdot \frac{1}{g_{mw}} \cdot \Delta f \quad (2.38)$$

If the *gate-referred* input noise voltage in strong inversion (Eqn. 2.34) is compared with the *gate-referred* input noise voltage in weak inversion (Eqn. 2.38) it can be seen that the transconductance g_m has a significant influence, because the terms $4kT$ and $2nkT$ are nearly equal for values of n in between $1 \leq n \leq 2$. Typical values of n are 1.5 to 1.8. Hence these terms can be assumed equal. The terms $(\frac{2}{3})$ and $(1 + e^{-\frac{V_{ds}}{V_T}})$ are also in the same range. Taking the worst case for $V_{ds} \approx 4V_T$ results in a value around 1. The inaccuracies of the first comparison and the second are mutually compensated. For an estimation, if the transconductance in strong inversion g_m is about 100 times larger than the transconductance in weak inversion g_{mw} it results in a $\sqrt{100}$ higher *gate-referred* input voltage noise for devices operating in weak inversion.

As a consequence the SNR (Eqn. 2.28) is about -20dB worse for circuits biased in weak inversion. In addition, if the supply voltage decreases for instance from 5V to 1V the SNR is then decreased by -27dB.

In low-voltage/low-power design white noise therefore becomes an important issue. Techniques in order to meet noise requirements of a system are

only given by careful handling of g_{mw} . It might be useful to drive the first amplifying stage at the interface between sensor element and the subsequent electronics in the moderate inversion region with large W/L ratios of the transistors, in order to find a compromise.

Devices which are switched off, have left the saturation region and equation 2.33 becomes invalid. The conductance G is in this case very small because the resistance R of a closed transistor is high. Noise can therefore be neglected for switched off devices.

Flicker Noise

Several studies relate to a type of noise that dominates at low frequencies. This kind of noise is called flicker noise or 1/f noise. As will be shown, the flicker noise is proportional to the inverse of the frequency. This is a relatively slow process and hence, this phenomena appears at low frequencies and introduces a further noise current at the drain of the transistor. Two dominant theories [35],[36]³ explain this phenomena. On the one hand they have different physical origins but on the other hand the resulting models are similar with respect to the design viewpoint. One theory [35] attributes flicker noise in MOS transistors to extra electron energy at the boundary between Si and SiO₂. The other theory is based on mobility fluctuations caused by carrier interactions with lattice fluctuations [37]. This work concentrates on the latter model that predicts an influence in the transition between the strong and the weak inversion region.

As previously discussed for the white noise, this noise current can also be transformed into a *gate-referred* noise voltage based on the correlation $i_d = g_m \cdot v_{gs}$. The resulting flicker noise voltage v_{fn}^2 ⁴ is expressed by

$$\overline{v_{fn}^2} = \frac{K(V_{gs})}{C_{ox}} \cdot \frac{1}{W \cdot L} \cdot \frac{\Delta f}{f} \quad (2.39)$$

In this equation 2.39 C_{ox} (gate capacitance per unit area) is a fixed parameter given by the technology and $(W \cdot L)^{-1}$ is given by the design. As a consequence the noise level can be influenced by W times L in the development process. This does not completely meet the requirement of the white noise, where the white noise depends on the ratio of W and L. Therefore W should be chosen as large as possible and for L a reasonable compromise

³These are only two exemplary citations for various publications related to this phenomena

⁴In SPICE the model [40] [41] is given by $\overline{i_{fn,ds}^2} = \frac{KF \cdot I_{ds}^{AF}}{C_{ox} \cdot L_{eff}^2} \frac{\Delta f}{f}$, where KF is the flicker noise coefficient, AF the flicker noise exponent, C_{ox} the gate capacitance per unit area, L_{eff} the effective channel length, f the frequency and I_{ds} is the drain current

must be found. But flicker noise is larger than white noise and hence L should at least not be chosen small in order to balance out both types of noise. With this technique flicker noise is reduced and white noise increased. The quantity $K(V_{gs})$ is bias-dependent as reported by [36]. In strong inversion $K(V_{gs})$ increases in an approximately linear fashion with $|V_{gs} - V_{th}|$ and in weak inversion $K(V_{gs})$ increases as $|V_{gs}|$ decreases. For simplicity's sake no distinction will be made between NMOS and PMOS transistors in this work, where NMOS transistors are rather independent of $|V_{gs}|$. As a result the $|V_{gs}|$ for low-voltage and low-power design should be chosen as close as possible to the threshold voltage in order to reduce the flicker noise.

The noise itself becomes worse the smaller the frequency and can be neglected for high frequencies due to $1/f$ in equation 2.39. Generally flicker noise in p-channel devices is significantly smaller than in n-channel devices for equal device dimensions.

In design practice p-channel devices are mostly chosen larger than n-channel devices in order to compensate the difference of the charge carriers mobilities. Hence noise is mostly determined by n-channel devices.

The meaning of the noise level in this work is given by the obtainable resolution qualified by the the signal to noise ratio as it is typical of all analogue systems. If the noise level is smaller than $1 \text{ mV} / \sqrt{\text{Hz}}$ the noise of the components would play a minor rule, because in mixed-signal systems the analogue signals are superimposed by noise caused by component switching of comparators and digital cells. This noise contribution is expected to be higher than the component noise. Hence the hysteresis of the comparators must be adjusted in respect of the highest noise source.

Concerning the aspired reduction of current and voltage within the components the input voltage noise becomes worse with smaller V_{gs} and therefore the SNR gets worse. Furthermore the reduction of the power supply voltage decreases the maximum signal range and worsens also the SNR.

2.2 Analogue Comparator

2.2.1 Simple Comparator

For basic investigations of comparators a conventional and simple topology with an additional node for biasing was at first chosen. Through this it was possible to drive the circuit in different modes, only by changing the supply current. In more complex circuits this is more difficult or only possible with limitations. By choosing the saturation points of the transistors at minimal levels, it was possible to apply smallest power supply voltages. For this the

The value of V_{ds} in equation 2.41 is larger than the saturation voltage of equation 2.40 and $V_{th} + V_{eff}$ is larger than V_{gs} of equation 2.40. Therefore the supply voltage must be increased for strong inversion operation.

If the circuit is biased in the weak inversion region, with some 10 nA, then saturation occurs at about $V_{dsat_{M5}} \approx 6 \cdot V_T \approx 150mV$. It is feasible to drive the input transistor below the threshold voltage due to the small bias current. From equation 2.7 the following equation 2.42 can be derived. It gives the dependencies for the minimum effective gate-source voltage $V_{eff} = V_{gs} - V_{th}$.

$$V_{eff} = n \cdot V_T \cdot \ln \left(\frac{I_D L}{I_S W} \right) \quad (2.42)$$

In the time domain simulation (Fig. 2.5) the drain current and the drain-source voltage of the current source M5 are depicted. Referring to a fixed reference voltage v_{ip} , the potential at the drain of M5 is adjusted to a minimum voltage of 150 mV. Smaller reference voltages or smaller signal voltages at vin would reduce this potential. In this case the current source would leave the saturation region.

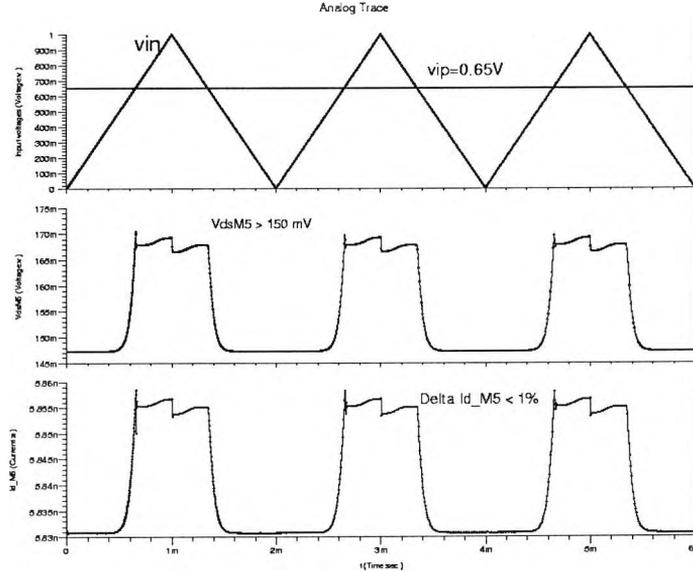


Figure 2.5: Time domain simulation of the simple comparator

The simulation result of figure 2.5 shows also the transition from the saturation region to the triode region. Assuming $n \approx 1.5$, $V_T = 150mV@25^\circ C$,

$\frac{W}{L} = 1$, a coefficient of the current ratio I_D/I_S of ≈ 0.1 and neglecting the channel length modulation, then V_{gs} of M1 can be calculated by equation 2.43.

$$V_{gs_{M1}} = n \cdot V_T \cdot \ln\left(\frac{I_D}{I_S}\right) + V_{th} \quad (2.43)$$

Based on these assumptions the input voltage is given by $V_{dsat_{M5}} + V_{gs_{M1}} \approx 150mV + 500mV \approx 650mV$. It can be observed that the circuit can operate with a slightly smaller input voltage, but this influences the current source, which results in slightly smaller currents of the current source. The current source is therefore no longer a stable source.

This type of comparator suffers from its relatively small common mode input voltage range, as is typical for single differential input stages, especially in low-voltage design such an input range is unacceptable. If for instance the power supply voltage is set to 1.2 V not even half of $V_{DD} = 0.6V$ is detectable which is very often an important detection point. Furthermore for the comparator a positive feedback, in order to accomplish the hysteresis, must be applied externally by resistors as it is well known from Schmitt-Triggers. In integrated circuit design this is not a good solution due to the die area that the resistors consume. As a result an advanced comparator must include an improved common mode input voltage range and in addition an internal positive feedback.

2.2.2 Advanced Comparator

2.2.2.1 Comparator Principle

Analogue comparators can in principle be designed by any traditional amplifier in an open loop configuration. But much effort in amplifier design is spent on achieving a good linearity. For nonlinear comparators the focus is different. The logic output should have a fast transition between two levels which is correlated with the gain. Therefore preamplification with a high gain is necessary. In order to enhance the input common mode voltage range a rail-to-rail input stage consisting of a p-channel and a n-channel differential pair must be used as depicted in figure 2.6.

Both the p-channel and the n-channel input stage generate a current depending on the input voltages. These currents must be combined by a summing circuit. In principle currents can be added taking Kirchhoff's current law into account, where two current sources supply the same node. After summation of the currents an electronic circuit part must decide which of the two remaining currents is larger. Track-and-latch circuits are popular due

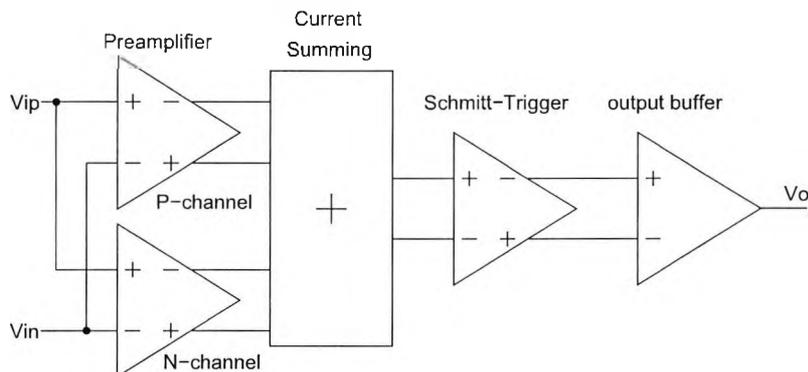


Figure 2.6: Comparator principle with a rail-to-rail input stage

to the positive feedback they apply in order to make the comparator very fast as for instance proposed in [47]. These circuits can perform a Schmitt-Trigger function that is known from conventional comparator design. With an output buffer, the Schmitt-Trigger circuit is isolated from the load of the comparator and a single-ended output stage is provided for the comparator.

For low-voltage and low-power design the supply currents must be kept small. Low-voltage operation is achieved if circuit parts operate at their minimum of stacked devices and if V_{gs} of the transistors are reduced to around V_{th} in moderate inversion or significantly below V_{th} in weak inversion operation. Furthermore, V_{dsat} of the current sources can be adjusted to be as small as possible for weak inversion operation down to $\approx 4 V_T$.

2.2.2.2 Preamplification and Summing Circuit

Input stages of comparators do not have to be different to input stages of differential amplifiers, nonetheless other concepts are used, as for instance comparators with switched capacitor auto-zeroing techniques [48] which consist of cascaded inverters. In this work comparators with rail-to-rail input capabilities are essential. Hence a differential comparator with a complementary input stage as introduced in section 2.1.5 must be used. The input circuit including biasing is depicted in figure 2.7.

Regarding the minimum power supply voltage range, no increase is given by the bias circuit which is smaller than that of the complementary differential input stage (Eqn. 2.27). With the current source I_b various currents can be applied for test purposes, so that all operation modes from weak to strong inversion are adjustable. In order to reach a high gain and to minimise offset and noise of the input stage large input transistors should be chosen. The

2.2.2.3 Schmitt-Trigger and Output Buffer

One of the most important functions of comparators in continuous time analogue design is hysteresis. For high gain and high speed comparators a very small amount of input noise is sufficient to generate output chatter. The topology of the cross coupled pair in figure 2.9 realizes a special gain stage.

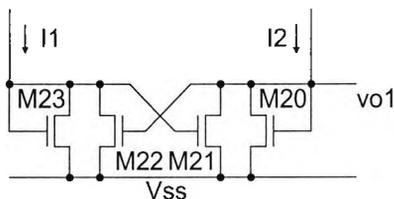


Figure 2.9: Gain stage with positive feedback [49]

If all current mirrors of the preamplification stage and the summing circuit have a ratio of 1 then $I1 = I2 = Ib$. Hence it can also be written [24]

$$I1 + I2 = 2Ib \quad (2.47)$$

Depending on the analysis [50] if $I1$ is increasing and $I2$ decreasing or vice versa at the crossover point the current relation is either

$$I1 = I2 \frac{(W/L)_{22}}{(W/L)_{20}} \quad (2.48)$$

or

$$I2 = I1 \frac{(W/L)_{21}}{(W/L)_{23}} \quad (2.49)$$

These currents also represent the drain currents of the input stage and the corresponding V_{gs} of the input devices can be calculated. Doing this, a difference between $V_{gs,n}$ for the negative input and $V_{gs,p}$ for the positive input is given and expresses a hysteresis. For $(W/L)_{20} = (W/L)_{23} = (W/L)_A$ and $(W/L)_{21} = (W/L)_{22} = (W/L)_B$ the hysteresis voltage V_{hys} is given by

$$V_{hys} = \pm \sqrt{\frac{2I_0}{k_p \left(\frac{W}{L}\right)_i}} \cdot \frac{1 - \sqrt{\frac{(W/L)_B}{(W/L)_A}}}{\sqrt{1 + \frac{(W/L)_B}{(W/L)_A}}} \quad (2.50)$$

The ratio of $(W/L)_B / (W/L)_A = \alpha$ determines the behaviour of the cross coupled topology. For $\alpha = 1$ the stage becomes a positive feedback latch which are used in discrete time architectures. If $\alpha < 1$ then the positive

feedback increases the gain and for $\alpha > 1$ the positive feedback performs a hysteresis and the circuit becomes a Schmitt-trigger [51]. Taking device variations into account an ideal latch function is never given. For the same reason the matching and therefore the device sizes of the cross coupled transistors must guarantee a reliable function in one mode.

At the output of the positive feedback circuit vo1 the transition between two voltage levels has a high gain. But these voltage levels do not range from VSS to VDD as is common for digital signals. Therefore a simple inverter realizes real digital output signals with typical CMOS levels. The inverting output buffer is depicted in figure 2.10.

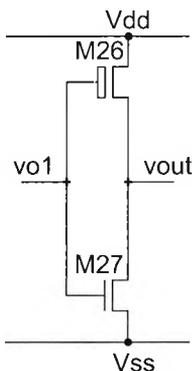


Figure 2.10: Output stage of the comparator

One further function of the output stage is to increase the overall gain of the comparator and with it the resolution of the comparator. In order to fit the device sizes of the inverter with respect to the input voltage level vo1, the input voltage at this node must be analysed. The switching point of the inverter should be centered around the voltage levels of vo1 which is generated by the current I_2 through the diode connected transistor M20 of the positive feedback circuit and depends on its V_{gs} . First the operation mode should be determined because the drain current of M20 is generated by the summing circuit transistors M24/M25. If any current amplification is given by the p-channel current mirror of figure 2.8 I_2 is larger than I_b . If, for instance, the input stage operates in the weak inversion region, then due to the current amplification the operation mode in positive feedback circuitry changes to moderate or strong inversion. Based on equation 2.11 which covers all regions of operation V_{o1} can be expressed by

$$V_{o1} = V_{th} + 2nV_T \ln \left(e^{\sqrt{\frac{I_2}{I_S} \cdot \left(\frac{L}{W}\right)^{2n}}} - 1 \right) \quad (2.51)$$

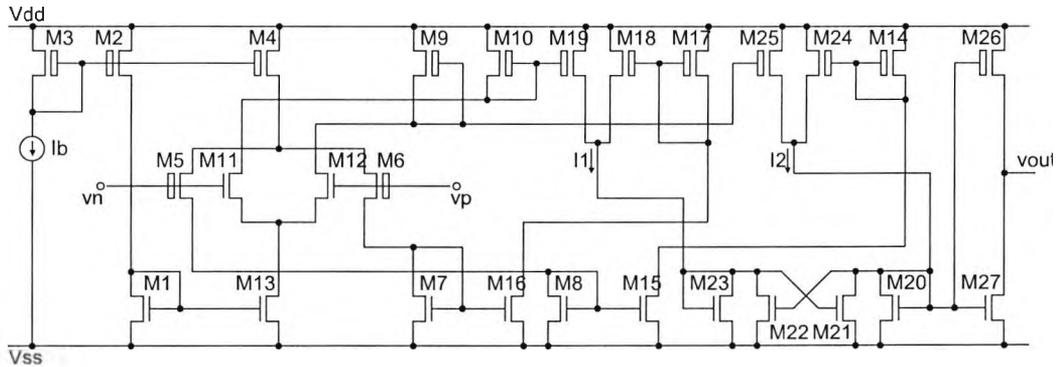


Figure 2.11: Rudimentary comparator schematic

I_2 can be between 0 and I_b or, if current amplification is applied in the summing circuit, x times larger than I_b . But for low-power design I_2 should not be enlarged significantly. If no current flows V_{o1} becomes zero.

Equation 2.51 can also be taken to determine the minimum power supply voltage for the circuit part. Only two devices are stacked where the p-channel devices act as a current source and therefore the saturation voltage of these transistors determine the operation range and the diode connected n-channel devices which operate at one V_{gs} . Hence the minimum power supply voltage is $V_{DD,min} = V_{gs} + V_{ds}$ which is two times smaller compared with the rail-to-rail input stage, if equal currents flow. Otherwise, if the current in the positive feedback circuit is much larger V_{gs} rises and can exceed the minimum power supply voltage of the rail-to-rail input circuit.

2.2.2.4 Rudimentary Comparator

Physical Design

The comparator has been realized in a 0.5μ CMOS technology where the n-channel and the p-channel transistors have threshold voltages of around 0.6 V and -0.6 V, respectively.

This comparator design is based on an origin of a bias current I_b of 100 nA, so that the most devices operate deep in the weak inversion region. Figure 2.11 shows the complete circuit with input stage, summing circuit, positive feedback, the output buffer and the bias circuit.

The input stage consists of a large differential transistor pair M5/M6 and M11/M12, in order to achieve a low voltage noise level at the input. They are supplied by two current sources M4 and M13, respectively, with bias currents that have similar values. The currents from the input stages are copied by

Device	W/ μm	L/ μm	Device	W/ μm	L/ μm
M1	2	2	M2	5	5
M3	5	5	M4	5	5
M5	200	0.5	M6	200	0.5
M7	4	4	M8	4	4
M9	50	4	M10	50	4
M11	500	3	M12	500	3
M13	3.5	3.5	M14	4	4
M15	4	4	M16	4	4
M17	4	4	M18	4	4
M19	50	4	M20	2	2
M21	2	2	M22	2	2
M23	2	2	M24	4	4
M25	50	4	M26	4	4
M27	0.6	0.5			

Table 2.1: Device dimensions of the comparator

some current mirrors with a ratio of 1 into the positive feedback stage. On the schematic level the positive feedback stage M20 to M23 has an ideal value of $\alpha = 1$ (page 28). The output stage M26/M27 realizes an output interface with CMOS voltage levels. Table 2.1 summarizes the device sizes.

Based on the device dimensions given in table 2.1 a layout has been developed. This layout is shown in figure 2.12. Each input transistor pair is matched by layout techniques in order to minimise stochastic offset. Within the finger structure the large input transistors are separated into several smaller transistors arranged in parallel. For the large current mirrors of the summing circuit on the right hand side of the layout a relatively good matching is also achieved.

This layout is suitable for standard cell layout design. With generous power supply terminals low wire resistances for the power supply are guaranteed. Guard banding techniques with well tied substrate connections minimise the distribution of noise via the substrate.

Measurement Results

A simple test-bench has been used for performance evaluation. This circuit is shown in figure 2.13. For the adjustment of the bias current I_b a resistor was chosen and at the output a small capacitance of 10 pF loads the circuit. The power supply and the reference voltages are generated by a stable refer-

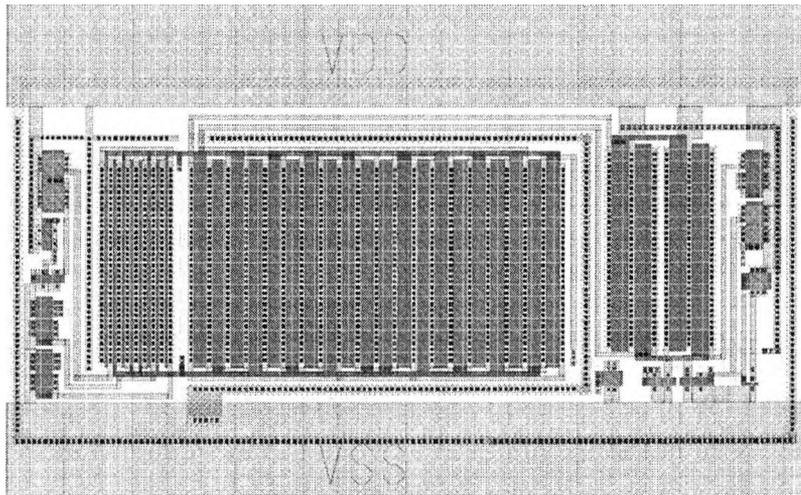


Figure 2.12: Comparator Layout

ence voltage. On the inverting terminal a function generator stimulates the integrated circuit cell.

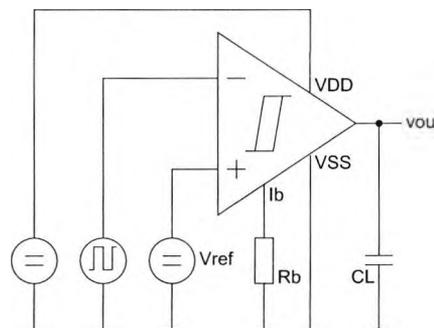


Figure 2.13: Testbench for the comparator

With this test bench the circuit behaviour in the time domain was evaluated by simulation and measurement. The measurement result in the following figure 2.14 depicts the numeric output of an oscilloscope. For comparison a simulation result generated by equivalent environment conditions is shown within the same figure.

The stimulation frequency of the square waveform is 70 kHz, the power supply voltage 1 V and the reference voltage is $V_{DD}/2$. Figure 2.14 shows that measurement and simulation results are approximately in congruence.

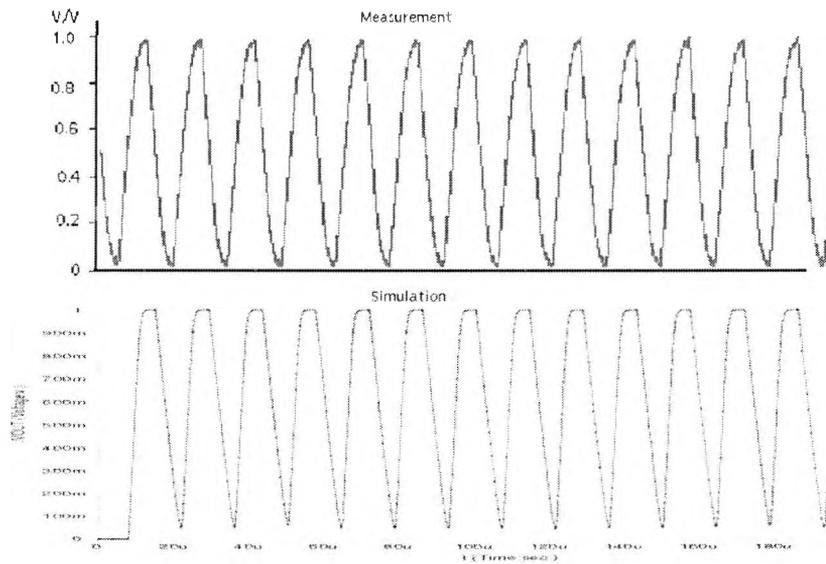


Figure 2.14: Comparison of measurement and simulation in the time domain

Input frequencies of about 50 kHz can be processed. In terms of the system requirements the comparator suffers from a slew rate, that is too small.

2.2.2.5 Comparator Optimization and Adaption

Overall Circuit

In sections 2.2.2 of this chapter the separate units of the comparator topology have been discussed. For the implementation several trade-offs are necessary in order to achieve best performance within the given general conditions of low-power and low-voltage. Important requirements for this design are

- low offset
- low noise
- high resolution
- high speed

The overall comparator circuit architecture is shown in figure 2.15. This circuit operates at 1.2 V power supply limited by the rail-to-rail input stage. In order to reach this a bias current of 250 nA is applied. As briefly discussed in section 2.2.2.4 smaller bias currents would allow smaller power supply

voltage e.g. with 100 nA a power supply voltage of 1 V. But in order to improve the speed of the comparator, a slightly higher bias current enables faster signal processing.

Offset in comparator design influences the resolution. In this work analogue signal processing is done without time discrete methods which employ oscillators for clock generation, because this would enlarge power consumption. As a consequence sophisticated solutions for offset cancellation cannot be used because they are based on switched capacitor technologies which need clocked signals. Offset is not scaled by the power supply and therefore the ratio between voltage signal range and offset voltage becomes worse. Hence the random offset must be kept small and systematic offset should be very small. The random offset is reciprocally proportional to the area of the transistors of the input stage. A model concerning the threshold voltage is given by [52], [53]

$$\Delta V_{th} = \frac{A_{V_{th}}}{\sqrt{WL}} \approx \frac{0.15t_{ox}}{\sqrt{WL}} \text{ mV} \quad (2.52)$$

where $A_{V_{th}}$ is a proportionality factor which is scaled down with the oxide thickness t_{ox} (unit in angstrom e.g. 100 Å).

A further correlation for the offset can be derived from the drain current equation in strong inversion operation. The offset voltage $V_{off} = V_{gs1} - V_{gs2}$ between two devices M1 and M2 is given by

$$V_{off} = \Delta V_{th} + \frac{\Delta\beta}{2\beta} \cdot (V_{gs} - V_{th}) \quad (2.53)$$

From equation 2.53 it can be concluded that for larger devices $\Delta\beta$ becomes small (and β large) and smaller overdrive voltages $V_{gs} - V_{th}$ will reduce the offset. Or in other words, larger drain-source currents generate larger offsets. Fortunately in low-voltage design the gate-source voltages are naturally small. But one shortcoming as a consequence of a rail-to-rail input stage is that both differential pairs contribute a separate non-correlated offset, with the result that in the worst case the input offset voltage of rail-to-rail input stages is two times larger if both input stages have equal device sizes. In addition the offset change over the common mode range will be in a nonlinear way. Keeping the offset small by large input device dimensions will also benefit the noise requirements.

Both input stage current sources take nearly the same current realized by current mirrors in the bias circuit with a ratio of 1. The dimensions of the input stage devices are listed in table 2.2. In order to adjust equal V_{gs} for input voltages of $V_{DD}/2$ the p-channel differential input transistor pair is 4 times larger.

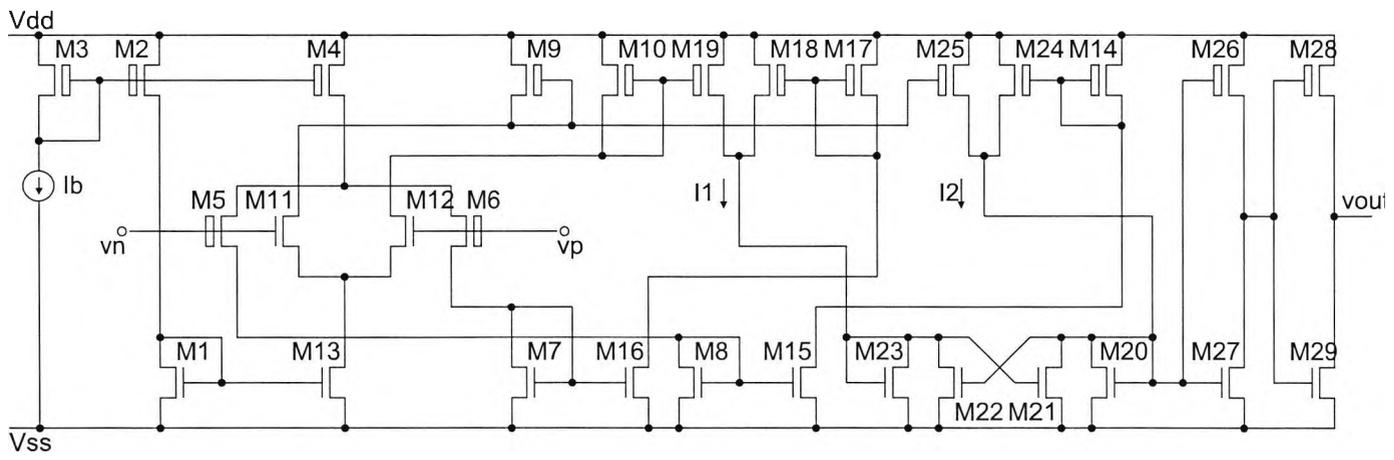


Figure 2.15: Overall rail-to-rail comparator

Device	W/ μm	L/ μm	Device	W/ μm	L/ μm
M1	2	2	M6	100	1
M2	2	2	M11	400	1
M3	2	2	M12	400	1
M4	5	5	M13	5	5
M5	100	1			

Table 2.2: Device dimensions of the comparator input stage

The summing circuit consists of six simple current mirrors. Improved current mirrors are not used due to the additional stack of voltages that would enforce larger power supply voltages. Large transistors are also required in respect of current matching. But on the other hand a large device causes a large parasitic capacitance which decreases the speed of the comparator. A moderate sizing of the devices is therefore suggested. One further problem must be considered for the sizing of the diode connected devices. As discussed in section 2.1.4 $V_{gs} = V_{ds}$ of these transistors can limit the common mode input range. For small W/L ratios V_{gs} increases and a thorough evaluation is necessary. Beside matching improvement by the device dimensions an increase of the effective voltage ($V_{gs} - V_{th}$) also improves current matching [55]. This correlation is given by

$$\frac{\Delta I_d}{I_d} = \frac{\Delta W/L}{W/L} - 2 \frac{\Delta V_{th}}{V_{gs} - V_{th}} \quad (2.54)$$

In order to achieve larger V_{gs} voltages the gate length of the diode connected transistors should be chosen large with respect to the width. Concerning the headroom for this increase of V_{gs} , V_{gs} may not exceed $V_{DD} - 2V_{dsat}$. The two saturation voltages are drain-source voltages of the current source and the input transistor. If those devices operate in the weak or moderate inversion region a total voltage drop of $\approx 2 \cdot 8V_T = 400mV$ must be at least available to prevent them from leaving saturation. Calculating L by using equation 2.11 gives

$$\frac{L}{W} = \frac{I_d}{2\mu C_{ox} n V_T^2 \cdot \ln^2 \left[1 + e^{\frac{V_{gs} - V_{th}}{2nV_T}} \right]} \quad (2.55)$$

For a given ($V_{gs} - V_{th}$) and a fixed current I_d the ratio of the device sizes can be calculated. Also a current amplification of 4 is adjusted. The transistor dimensions are listed in detail in table 2.3.

Device	W/ μm	L/ μm	Device	W/ μm	L/ μm
M7	5	2	M8	5	2
M9	5	1	M10	5	1
M14	5	1	M15	5	2
M16	5	2	M17	5	1
M18	10	0.5	M19	10	0.5
M24	10	0.5	M25	10	0.5

Table 2.3: Device dimensions of summing circuit

This comparator is used in a noisy environment. In addition to device noise, substrate noise, noise on the power supply and the sensor noise as well as magnetic noise from the environment measured by the sensor, contribute to the disturbances in the system. Common mode signals will be rejected by the differential input stage. Perturbation must not occur as a common mode signal and therefore small differential signals will be amplified and can cause comparators to chatter at the output. Positive feedback can drive an amplifier for very small signals into saturation so that the output clips either at V_{DD} or V_{SS} . But the positive feedback can be applied in such a way that the comparator behaves like a Schmitt-trigger with hysteresis. In order to adjust the hysteresis on a design level the noise at the comparator input must be estimated. It is one difficulty of this work to determine the total amount of voltage disturbance in the system. The device noise has been discussed in section 2.1.6.

For a rough estimation of device noise at the input of the comparator, the white noise and the flicker noise can be calculated. Assuming that the input transistors operate in weak inversion (based on equation 2.9) and $I_d = 250nA$, $n = 1.6$, $g_{mw} = 6\mu A/V$, $T = 300^\circ K$, the $KF = 3.7e - 28$ and $t_{ox} = 100 \text{ \AA}$, applying equations 2.35 and 2.39 gives a gate-referred white noise of $47 \text{ nV}/\sqrt{Hz}$ and a flicker noise for 1 Hz of $558 \text{ nV}/\sqrt{Hz}$. The total noise can be obtained by integration over the bandwidth of interest.

In addition to the calculated input noise of the comparator input devices the noise voltages at the interface have to be taken into account. Within this work the comparator is used for two different tasks. For the voltage comparison inside the folding unit the amplified input noise of an operational amplifier determines the noise density at the interface. At the interface of the comparator within the A/D converter two separate noise sources exist. One coming from the reference voltage at one node of the comparator and the other node the equivalent resistance at the tap of the resistor string

determines the noise density. Intentionally only one comparator is designed for multiple usage - adapted to that interface with the highest noise.

Assuming that the total noise caused by the components and elements is smaller than 1 mV the noise generated in a mixed-signal circuit would dominate. The other system based noise sources are less determinable compared with the noise analysis of the components and elements. A reasonable value is larger than 1 mV. For this work a hysteresis of ± 2.5 mV is chosen.

The adjustment of the positive feedback circuitry in order to achieve hysteresis is discussed in section 2.2.2.3. Hysteresis is commonly related to V_{gs} of the input devices. Based on the input device size ratio $(W/L)_i$ and I_d the inversion level can be determined. For the given drain current of $250/2$ nA for each input transistor and geometries of $100 \mu m$ to $1 \mu m$ for the n-channel transistor, the devices operate in the deep weak inversion, if for example, the specific current is 411 nA. Supposing for simplicity's sake that only the n-channel input stage is active, then the hysteresis relates only to one input pair. The hysteresis voltage V_{hys} can be calculated by the difference of V_{gs} of the input devices. Calculating V_{gs} from equation 2.7 and subtracting V_{gs} of both transistors leads to

$$\alpha = e^{\frac{|\pm V_{hys}|}{nV_T}} \quad (2.56)$$

where $\alpha = \frac{(W/L)_{22}}{(W/L)_{20}} = \frac{(W/L)_{21}}{(W/L)_{23}}$. For a hysteresis of $\pm 2.5 mV$ a ratio of 1.06 for the transistor pairs would generate the desired hysteresis. Taking matching problems, process variation and the parasitic capacitances of the positive feedback stage into account, leads to a trade-off for the device sizes listed in table 2.4

Device	W/ μm	L/ μm	Device	W/ μm	L/ μm
M20	5	5	M21	6	5
M22	6	5	M23	5	5
M26	5	0.5	M27	5	0.5
M28	20	0.5	M29	5	0.5

Table 2.4: Device dimensions of the positive feedback stage

An important aspect that has not yet been considered is the temperature dependence of the hysteresis. If the same hysteresis should be guaranteed at -40° , α must be increased up to 1.08. The hysteresis will increase at $+120^\circ$ up to 4.2 mV.

The output buffer consisting of M26 and M27 is sensitive to the output voltage $vo1$ of the positive feedback stage. Due to the diode connected device

M20 the voltage range at this node is $0 \leq v_{o1} \leq V_{dsat,M20}$. Hence the switching point of the inverter must be within this voltage range. It is an issue that must be considered with respect to stability because for small device sizes the process variation may cause a bad yield. In order to achieve stability the following aspects must be taken into account.

- v_{o1} or $V_{gs,M20}$, respectively, can be slightly enlarged by a small W/L ratio.
- v_{o1} must be larger than V_{th} to switch on M27.
- M27 could be switched on permanently, depending on the power supply and threshold voltages.
- M20/M27 act as a current mirror.
- output drive capability depends on V_{gs}
- propagation delay depends on V_{gs} and W/L

The switching point v_{sp} corresponds to the point when the input voltage is equal to the output voltage. For strong inversion operation as well as for weak inversion both transistors are saturated at the switching point. Assuming that both transistors operate in the strong inversion region and the drain currents of each transistor is equal allows the following expression for the inverter.

$$\frac{1}{2}\beta_n(v_{sp} - V_{th,n})^2 = \frac{1}{2}\beta_p(V_{DD} - v_{sp} - V_{th,p})^2 \quad (2.57)$$

Solving this equation with respect to v_{sp} gives

$$v_{sp} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{th,n} + V_{DD} - V_{th,p}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \quad (2.58)$$

With equation 2.58 the switching point can be centered around $V_{DD}/2$. The device sizes are listed in table 2.4.

Simulation Results

In the previous chapter the overall circuit was introduced. The comparator simulation test bench is equal to the test bench in figure 2.13. At the non-inverting input a fixed reference voltage is applied. For this comparator consisting of a rail-to-rail input stage this reference voltage can be in a wide

range very close to both power supply voltages. At the inverting terminal of the comparator various stimuli for large signal and time domain analysis have been applied. The power supply voltage was 1.2 V and the bias current 250 nA. The output was permanently loaded by 10 pF.

Figure 2.16 shows the simulation result for various overdrive voltages at the input. The smallest overdrive voltage is limited by the hysteresis. In order to guarantee operation over a range of temperature the smallest overdrive voltage was chosen at 5 mV.

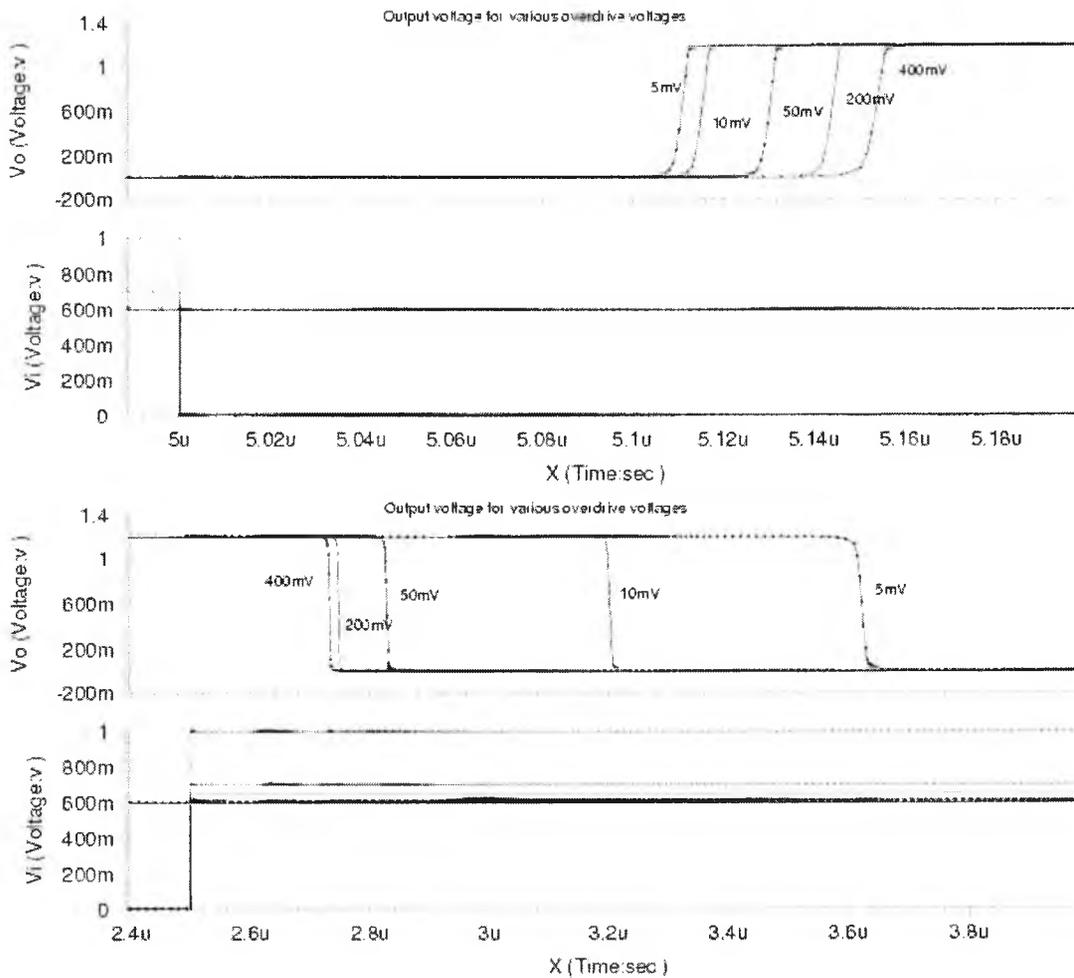


Figure 2.16: Propagation delay falling edge for various overdrive voltages

As expected, the propagation delay decreases with increasing overdrive voltages. The propagation delay on the falling edged is much worse than on rising edge. Driving the comparator with a symmetric overdrive voltage with

respect to reference will generate approximately equal propagation delays on rising and falling edges. The propagation delay depends on the direction and the voltage value of the input signal. This does not represent the actual operating conditions. Hence this simulation shows the worst case evaluation for the circuit.

Stability considerations on electronic circuits include temperature dependencies among others. The following figure 2.17 depicts the influence of the temperature on the propagation delay. The results are based on the previous stimulation with an overdrive voltage of 5 mV.

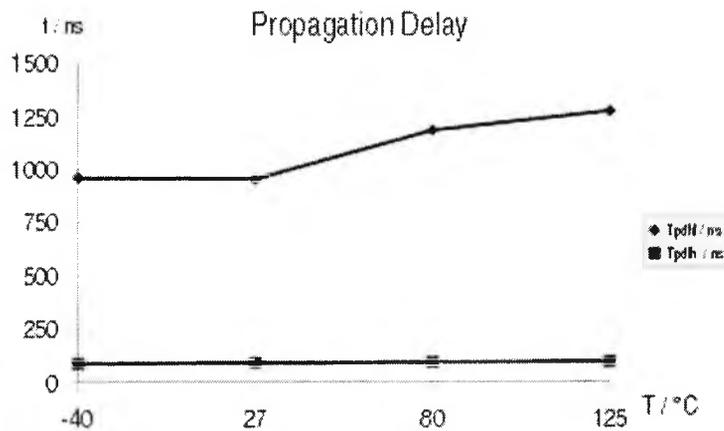


Figure 2.17: Propagation delay vs. temperature

Over the temperature range the propagation gets worse with increasing temperature. This is expected because the drain currents decrease with increasing temperatures due to an increase of V_T (Eqn. 2.7). An increasing V_T lowers also the gain because g_m becomes smaller.

In order to find a compromise for the supply current, the propagation delay was investigated for miscellaneous bias currents for a 1.2 V power supply voltage. The result is shown in figure 2.18.

The simulation result shows that 250 nA is a good trade-off between speed and power consumption because for higher bias currents the gained speed predicts a convergence. Only much more bias current, by increasing power supply voltages, will improve the circuit behaviour.

The hysteresis of the comparator also depends on the temperature. The reasons are discussed above. Table 2.5 includes the results over a temperature range of -40 to 125 degree.

An increase of the hysteresis over the temperature range has to be taken into account for the resolution of the system which is influenced by the hys-

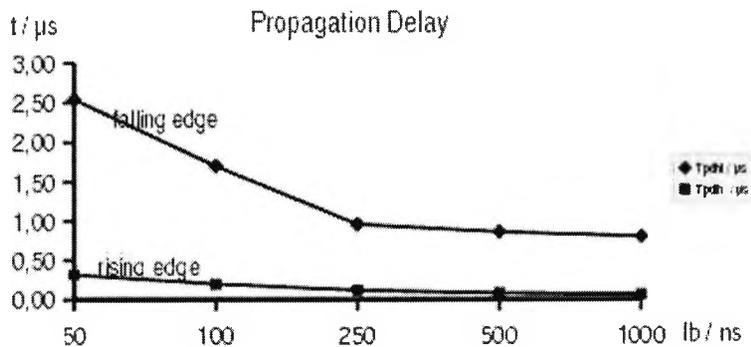


Figure 2.18: Propagation delay vs. bias current

teresis. In practice perturbation will increase also over temperature. An increase of hysteresis will therefore be good for stability.

Table 2.6 summarizes the characteristics of the comparator. Unless otherwise noted the conditions are 27 degree room temperature, 250 nA bias current, 1.2 V power supply voltage, no load resistance and 10 pF load capacitance.

With 4.3 μW is the comparator well suited for low-power operation. The performance is comparable to commercial products, taking into account that a rail-to-rail input stage consumes two times more current than a single input stage.

Regarding the simulation and measurement result of figure 2.14, the time domain simulation of this optimised comparator shows exactly the same behaviour at a frequency of 5 MHz and 1.2 V power supply voltage. This is a significant increase in performance.

Temperature	$\pm V_{hys}$	offset	unit
-40	2.5	0.7	mV
27	3.2	0.4	mV
80	3.7	0.1	mV
125	4	0.1	mV

Table 2.5: Temperature effects on hysteresis

Parameter	Symbol	Value	Unit	Conditions
Supply voltage	V_{DD}	1.2 to 5.5	V	
Supply current	I_{DD}	3.6	μA	no load
Temperature range	T_A	-40 to 120	deg	
Input offset	V_{io}	400	μV	systematic
Input common mode range	$V_{i,cm}$	0.02 to $V_{DD}-0.02$	V	$V_{DD} \geq V_{DD,min}$
High level output voltage	V_{oh}	1.2	V	no load
Low level output voltage	V_{ol}	0	V	no load
Propagation delay				$C_l=10$ pF,
Rising edge	$t_{pd,lh}$	1.1	μs	$V_{overdrive}=5mV$
Propagation delay				$C_l=10$ pF,
Falling edge	$t_{pd,hl}$	0.15	μs	$V_{overdrive}=5mV$
Fall time	t_f	5.2	ns	$C_l=10$ pF
Rise time	t_f	7.1	ns	$C_l=10$ pF
Fixed hysteresis	V_{hys}	3.2	mV	@27 degree
DC gain	A_D	80	dB	

Table 2.6: Characteristic of the comparator

2.3 Differential Amplifier

2.3.1 Input Stage

2.3.1.1 Common Mode Input Range

Differential amplifiers in low voltage applications have, due to the reduced power supply voltage, a smaller voltage range within which signal processing is possible. In order to maximize the range of signal processing at the input of the amplifier, rail-to-rail input stages are typically used. Such input stages consist of a complementary PMOS/NMOS differential transistor pair.

However, the rail-to-rail input stages are not necessary in every case. Consider the operational amplifiers in figure 2.19. The inverting a) and non-inverting b) OPAMPs tend to have very small signals at the input and these should be amplified. Hence the applied signal at the input stage needs only very small portions of the input range. A single NMOS or PMOS input stage may be sufficient. One advantage can therefore be that the power supply voltage of only one V_{gs} and one V_{ds} is necessary (Eqn. 2.26). But requirements on the DC-level may limit this advantage because very often the DC-level is set to around half of the power supply voltage. An increase of the power supply voltage would be the result. Nevertheless some effort in

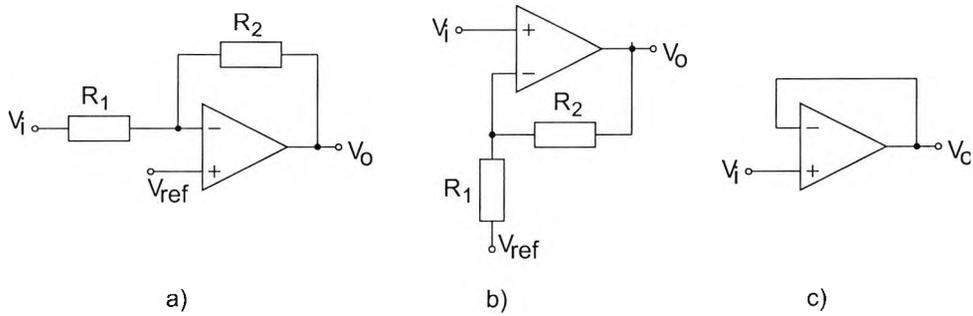


Figure 2.19: Operational amplifier configurations

design and smaller chip area can be gained if only a single input stage is used in spite of increasing the power supply voltage due the operating point given by the sensor. OPAMPs used as voltage followers (Fig. 2.19c) have typically large signals at the output as well as at the input. In this case a rail-to-rail input stage is necessary.

The proceeding considerations concentrate on rail-to-rail input stages as an universal input interface. Basically, signal processing is possible over the complete voltage range at the input between both power supply voltages, if a minimum power supply voltage is guaranteed. A rail-to-rail input stage consists of a complementary differential input transistor pair M1/M2 and M3/M4 as depicted in figure 2.20.

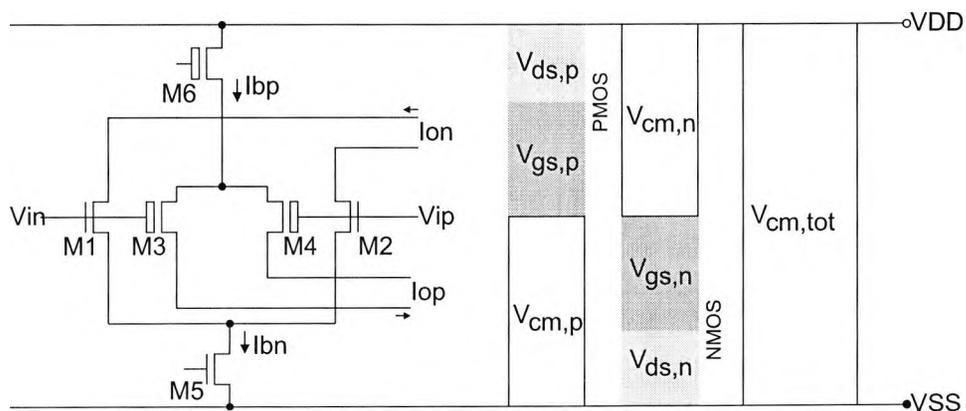


Figure 2.20: Common mode range of a rail-to-rail input stage

The common mode voltage range of the overall input stage is determined by the supply voltages and not by the sum of both common mode voltage ranges of the differential pairs.

$$V_{cm,tot} = V_{dd} - V_{ss} \quad (2.59)$$

In order to obtain this function without a gap in signal processing the following conditions have to be fulfilled.

$$V_{cm,p} \geq V_{gs,n} + V_{ds,n} \quad (2.60)$$

$$V_{cm,n} \geq V_{gs,p} + V_{ds,p} \quad (2.61)$$

The minimum power supply voltage is given by equation 2.27 if the common mode voltages are equal to $V_{gs} + V_{ds}$ and if $V_{gs,n} = V_{gs,p} = V_{gs}$ and $V_{ds,n} = V_{ds,p} = V_{ds}$.

V_{gs} of the input transistor is determined by the current, due to the strong correlation between the drain current and the gate source voltage (Eqn. 2.3 and 2.7). If the drain current I_d is ten times smaller than the specific current I_s the transistor operates in the weak inversion region and $V_{gs} \leq V_{th}$. The maximum current is adjusted by the current source that conducts a mirrored reference current.

2.3.1.2 Current Sources

Each transistor pair is supplied by a separate current source. Without any restrictions on the power supply voltage such current sources would be realized by high-swing cascode current sources which have a very high output impedance. But high-swing current mirrors would enlarge the minimum power supply voltage by one V_{dsat} at a minimum for each current source of the rail-to-rail input stage and in most cases increase power consumption due to one additional current source that is needed to bias parts of the high swing-cascode. The main benefit of cascoded current sources is the enlarged output impedance.

On the other hand if a single transistor operates as a current source in the weak inversion region the output impedance is equal r_{ds} and is naturally very high. Recalling equation 2.18 shows that for large drain-source voltages the output conductance becomes extremely small and therefore the output resistance extremely high. For instance, at room temperature, for a current of 500nA and $V_{ds} = 150mV$ the output impedance is $16M\Omega$ and increases substantially with larger drain-source voltages. The worst case for saturation is about $4\dot{V}_{ds} \simeq 100mV$ at room temperature. The minimum output impedance is then approximately $2M\Omega$. As a result a single transistor operating in weak inversion is sufficient for the current sources of the rail-to-rail input stage as depicted in figure 2.20 if they are biased in the weak inversion region.

2.3.1.3 Differential Input Transistor Pair

Figure 2.20 shows the topology of the rail-to-rail input consisting of two complementary differential pairs. Basically, each transistor pair operates inside a region until the current source becomes unsaturated. The operating regions of both have to overlap in the common mode range.

Different issues refer to the dimension of the transistors. One of them is the gain A of the input stage which is proportional to the transconductance g_m of the transistors and the load resistance R_L , as given by

$$A = g_m \cdot R_L \quad (2.62)$$

Hence, a high transconductance g_m is desired in order to maximize the gain. For devices operating in the strong inversion region $g_m^2 \propto W/L$ (Eqn. 2.15) a good reason exists to make W/L ratio large. But g_m in weak inversion operation is proportional to I_d (Eqn. 2.17) and is independent of the dimensions. In order to realize a high gain drain current I_d should be as large as possible and R_L as large as possible. But I_d is limited to about the tenth of the saturation current I_s or the differential pairs are operating with a larger current in the moderate or strong inversion region. The moderate inversion might be a good compromise.

An advantage of a large open-loop gain is that the amplifier gets a high stability. This stability against component characteristics, aging, temperature etc. is also called desensitivity D . The amplification with feedback is expressed by the definition

$$A_f = \frac{A_0}{1 + \beta_f A_0} = \frac{A_0}{D} \quad (2.63)$$

were A_f is the gain with feedback, A_0 the open-loop gain (without feedback), β_f the transmission factor for the feedback network and D the desensitivity. If $\beta_f A_0 \gg 1$ then

$$A_f = \frac{A_0}{1 + \beta_f A_0} \approx \frac{A_0}{\beta_f A_0} = \frac{1}{\beta_f} \quad (2.64)$$

That means that for a high desensitivity the amplification depends on the transmission factor β_f which is often a negative real number but can also be a complex function of the signal frequency. If for example $A_0 = 70dB \simeq 3000$ and $1/\beta_f = 30$ the influence of variations of A_0 is $\approx 1\%$ and for $A_0 = 90dB \simeq 30000 \approx 0.1\%$. Hence a high open-loop gain is desired.

As noticed, a large W/L does not improve the gain of an input differential pair that is working in the weak inversion region (Eqn. 2.17). For the same reason, the transconductance in weak inversion g_{mw} does not depend on the

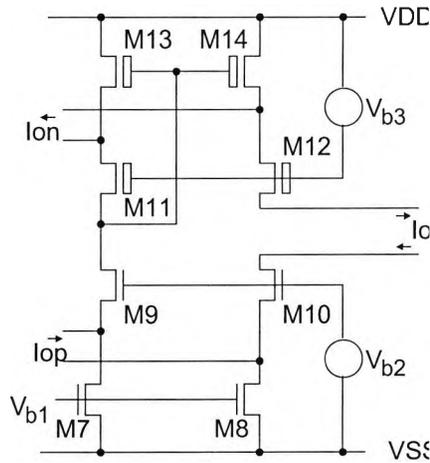


Figure 2.21: Active load for the rail-to-rail input stage

device dimensions, so no compensation between PMOS and NMOS transistors is necessary as is the case for devices working in strong inversion where the mobility μ for both transistor types is different, resulting in different sizes of the transistor pairs.

One reason that the device sizes should not be kept too small is that the flicker noise for the input transistor pairs can be reduced. Both W and L should be large. On the other hand large input transistors consume chip area. Therefore the device dimensions can not be enlarged very much. Furthermore, large input devices would also increase the input capacitance that would result in a pole at lower frequencies.

2.3.1.4 Active Load

Rail-to-rail input stages need to have a load that combines the current of the p-channel and the n-channel input stage. Diode-connected transistors which mirror the current out of the input stage would prevent rail-to-rail operation at the same power supply voltage because a diode connected transistor needs one V_{gs} for operation. For low voltage applications it is therefore mandatory to apply a folded cascode load. Various advantages exist with such a load. The first, as previously mentioned, is the common mode voltage input range. The second is that a large gain can be realized due to the large impedance at the output node.

The active folded cascode load for the rail-to-rail stage is depicted in figure 2.21.

At the input, the output currents I_{on} and I_{op} of the rail-to-rail input

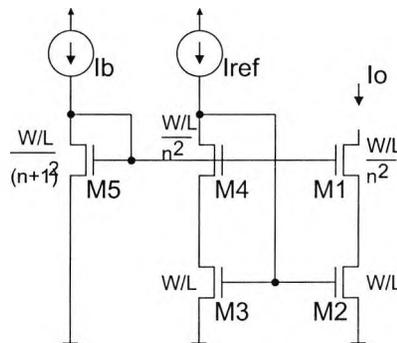


Figure 2.22: Wide-swing current mirror

stage flow into the folded cascode load circuit. This circuit is a summing circuit for the currents where the total current flows through M7 and M13, respectively. Each input pair is supplied by separate current sources I_{bn} and I_{bp} (Fig. 2.20). For $I_{bn} = I_{bp} = I_{ref}$ the total current should be chosen as $2I_{ref}$ in order to maximize the output current. For weak or moderate inversion V_{gs} of M7 and M8 is smaller than V_{th} . Particularly in weak inversion V_{ds} can be as small as possible at about $4V_T$.

M9 and M10 are used in a common-gate configuration, if they are biased by a fixed voltage V_{b2} . In conjunction with the p-channel input stage these transistors operate as a folded cascode. The dimensions of the transistors are less critical and can be kept small. More important is the bias voltage which determines the operating range of M7 and M8, respectively.

For OPAMPs with a single instead of a fully differential output a differential to single ended conversion must be done. Comparable with a simple Miller OPAMP this conversion is also done by a current mirror. The output impedance of a simple current source operating in the strong inversion region is $r_d \cong 1/(\lambda \cdot I_d)$. Values of some $M\Omega$ are typical. If the influence of the drain-source voltage across the current source must be reduced, an improved current source is necessary. Different types of improved current sources are known [23], [24]. Some concepts are improved in respect of a minimum drain-source voltage in order to maximize the swing. Several hundred mega ohms are possible for the output impedance of current sources with advanced techniques. The principle of an improved wide-swing current mirror [43], [42] is shown in figure 2.22.

Wide-swing current mirrors are also called low voltage current mirrors. The reason is that the voltage drop across M1/M2 can be adjusted to a minimum of

$$V_o \geq (n + 1) \cdot V_{dsat} \quad (2.65)$$

where n is a positive-integer number which should be simply one for low voltage applications in order to operate the circuit at the lowest possible power supply voltage. An advantage compared with other wide-swing current mirrors is that V_{ds} of M2 and M3 in figure 2.22 is matched with a very high accuracy. Hence no channel length modulation problems exist which results in an extremely high current matching. This is necessary because current mismatching causes offset.

Therefore if this wide-swing current mirror is used for the differential to single ended conversion within the active load of the rail-to-rail input stage an improved current matching will lead to less offset.

Another property of the wide-swing current mirror inserted within the active load is used. As shown in figure 2.21 a current summation node exists for the n-channel differential input between the source of M11 and the drain of M13. Due to the fixed bias voltage of M11 and M12 these transistors operate similarly to M9 and M10 because they also operate as a common-gate amplifier. This low-voltage current mirror does therefore not impede rail-to-rail operation. In conjunction with the n-channel input stage the low-voltage current mirror forms a folded cascode stage.

2.3.1.5 Input Transconductance

One drawback exists if a complementary rail-to-rail input stage in the configuration of fig. 2.20 is used. Within the common mode input range the transconductance of the input stage changes by a factor of two [31]. This results in signal distortion and an inconstant unity-gain bandwidth.

The problem of the variations in the transconductance is shown in figure 2.23 where the normalized transconductance of the NMOS and the PMOS transistor is shown. If both transconductances are added the total input transconductance is $g_{m,tot}$ which changes by a factor of two. Some techniques for controlling the transconductance are proposed in [31] resulting in transconductances that change only by some percent.

An example for the distortion is based again on equation 2.63. If $A_0 = 70dB \simeq 3000$ and $1/\beta = 30$ and the transconductance varies by a factor of two, the ratio of V_{out}/V_{in} changes by $\approx 0.5\%$. But if the open-loop amplification is increased ten times up to $90dB$ the changes are less than 0.05% which is practically negligible. The change in the unity-gain bandwidth always obeys

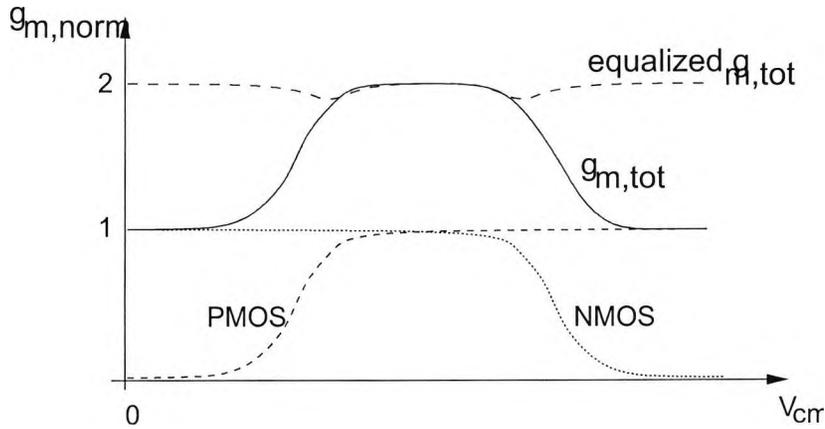


Figure 2.23: Total input transconductance

$$\omega_t = \frac{g_{mi}}{C_M} \quad (2.66)$$

where ω_t is the transition per unity-gain bandwidth, g_{mi} total transconductance of the input stage and C_M is the Miller capacity which is used in compensated OPAMPs. Taking into account that the transconductance of the input stage varies by a factor of two results in a proportional dependence of ω_t .

2.3.2 Output Stage

Various types of output stages are used in amplifier design. A thorough characterization with respect to system requirements is important so as to decide on the right type. In low power applications it seems to be a good solution to make use of the ability of a class-B output stage with very low quiescent current and a power efficiency of 75% for a rail-to-rail output sine wave. Characteristic for this kind of output stage is also a significant signal distortion which is a very large signal range at the output in respect to low-voltage amplifiers. For most measurement applications this high distortion is unacceptable, because the system accuracy is significantly reduced.

A class-A amplifier is also unsuitable because a static current flows all the time in the drain of the transistor depending on the operating point. The maximum output current of a class-A amplifier is the quiescent current. For a rail-to-rail sine wave a power efficiency of only 25% is achieved which is quite small.

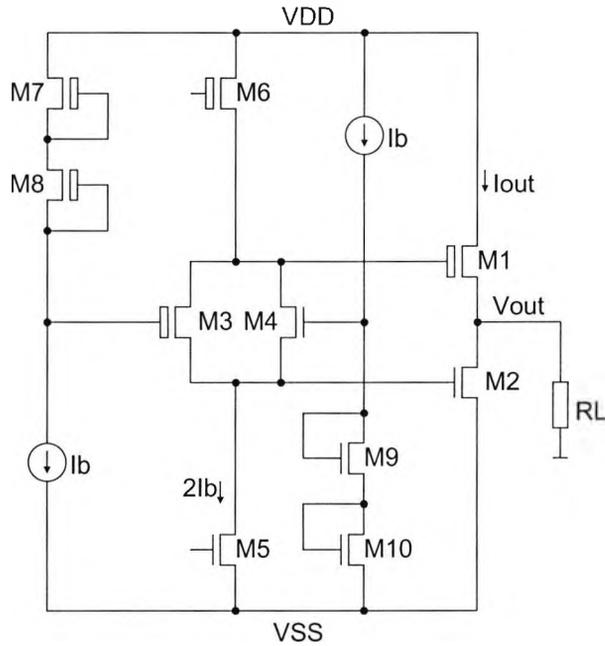


Figure 2.24: Feedforward class-AB output stage

A suitable solution is a complementary common-source configuration biased in class-AB mode. This is a compromise between class-A and class-B operation. If the complementary push-pull stage is biased in the right way, the crossover distortion of class-B mode can be minimised. Typical for class-AB operation is that a small standby current flows at zero excitation. As a result, more power dissipation is necessary compared with class-B mode, but on the other hand the signal distortion is tolerable.

Output amplifier principles with complementary common-source or source-follower configuration that work in the class-AB mode have to be biased. Two types of biasing are used for this purpose - feedforward class-AB output stages or feedback class-AB output stages [31]. For this work a feedforward class-AB output stage as depicted in figure 2.24 was used.

This approach of a class-AB output stage needs a minimum power supply voltage which is given by

$$V_{dd,min} = 2V_{gs} + V_{ds} \quad (2.67)$$

if $V_{gs,n} = V_{gs,p} = V_{gs}$. This is valid for all branches of the circuit. M1 and M2 are the push-pull output devices operating in a complementary common-source configuration and M5 and M6 are typical gain stages. The transistors M3 and M4 are arranged as common-gate level shifters in order to spread

the voltage between the output devices M_1 and M_2 . With two in series diode-connected transistors M_7/M_8 and M_9/M_{10} , respectively, the fixed gate voltages for the level shifters are set. Given the condition that $(W/L)_3 = (W/L)_8$ and $(W/L)_4 = (W/L)_9$ the gate-source voltage drop at M_1 and M_7 as well as M_2 and M_{10} are equal and the output current I_{out} obeys

$$I_{out} = I_b \frac{(W/L)_1}{(W/L)_7} = I_b \frac{(W/L)_2}{(W/L)_{10}} \quad (2.68)$$

The relationship between the other transistors, for the case that the currents through M_7/M_8 and M_9/M_{10} are equal (I_b), can be given by

$$\frac{(W/L)_7}{(W/L)_{10}} = \frac{(W/L)_8}{(W/L)_9} = \frac{(W/L)_3}{(W/L)_4} = \frac{(W/L)_1}{(W/L)_2} = \frac{\mu_p}{\mu_n} \quad (2.69)$$

One major property of the output stage of figure 2.24 is a rail-to-rail behaviour. The output signal swing reaches nearly both power supply rails. For strong inversion operation the minimum and maximum output values can be calculated. Based on equation 2.1 (neglecting V_{ds}^2) when the transistor leaves the saturation and enters the triode region the output range can be estimated by

$$V_{DD} \frac{1}{2(1 + \beta_n V_{eff,n} R_L)} \leq V_{out} \leq V_{DD} \left(1 - \frac{1}{2(1 + \beta_p V_{eff,p} R_L)}\right) \quad (2.70)$$

where $\beta = \mu C_{ox} W/L$, $V_{eff} = V_{gs} - V_{th}$, $V_{SS} = 0$ and R_L is the load resistance. It can be concluded that the higher the load resistance, the larger the output range becomes. For weak inversion the equation is not explicitly solvable. Nevertheless the influence of the load resistance is similar.

2.3.3 Rudimentary OPAMP

The OPAMP has been realized in a 0.5μ CMOS technology where the n-channel and the p-channel transistors have threshold voltages of around 0.6 V and -0.6 V, respectively.

The previously described techniques of rail-to-rail input/output stages are taken for the design of a low-voltage and low-power amplifier. Apart from the major requirements of a minimum power supply voltage and a minimum necessary power consumption, important details for design are properties such as

- low noise,

- low offset,
- high unity-gain bandwidth,
- high open-loop gain,
- large common-mode input range,
- large output swing,
- output drive capabilities,
- small die area.

These are a lot of items, with in some cases conflicting requirements like low offset and small die area. Hence compromises must always be found based on the fixed major requirements.

In order to evaluate the performance of the measurement system of this work only one basic type of amplifier was developed. In application specific integrated circuits several types of amplifiers, each optimised for different tasks, would normally be inserted. Special amplifiers with for instance different input or output circuits could be fitted at each position inside the system which could entail a performance improvement. Nevertheless with an universal amplifier the principle can be shown.

The universal amplifier consists of a rail-to-rail input stage with g_m -control circuit and a wide-swing class-AB output stage. This output stage must be able to drive capacitive as well as resistive loads, which results in an amplifier shown in figure 2.25.

As described in section 2.1.5 the unequal mobilities of charge carriers μ_n and μ_p lead to different sizes of the input transistors. The relation is given by

$$\frac{(W/L)_p}{(W/L)_n} = \frac{\mu_n}{\mu_p} \quad (2.71)$$

In detail the sizes of the input stage transistors are shown in table 2.7.

Device	W/ μm	L/ μm	Device	W/ μm	L/ μm
M1	400	3	M4	100	3
M2	400	3	M5	10	3
M3	100	3	M6	10	3

Table 2.7: Device dimensions of the input stage

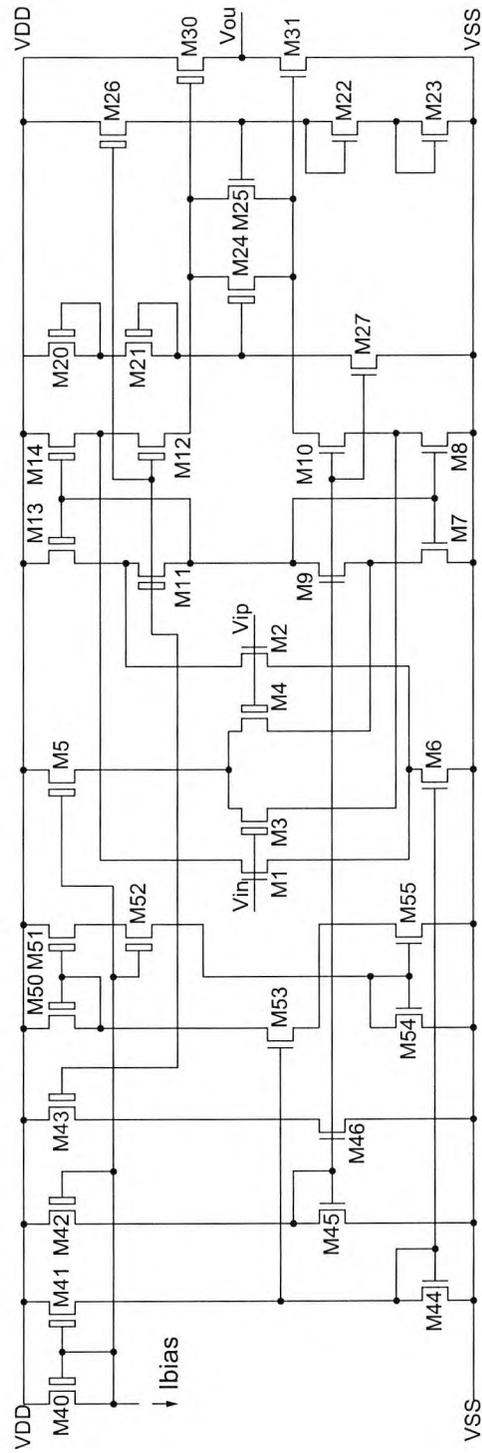


Figure 2.25: Schematic Rail-to-Rail Input/Output Amplifier

The current sources are driven by the current mirrors M40/M5 and M44/M6. At the node *Ibias* an external current is applied which can be generated in a very simple way by a resistor connected to VSS. This is only done for testing in order to be able to apply different currents and to drive the amplifier in different modes.

The dimensions of the current sources M5 and M6 have been chosen to be equal. For currents in the weak inversion region, the slope factors n and the W/L ratio are equal, a difference of V_{gs} occurs which can be expressed by $\Delta V_{gs} \simeq n \cdot V_T \cdot \ln \frac{I_{s,p}}{I_{s,n}}$. With $n \approx 1.7$ and a ratio of the saturation currents I_s for p-channel and n-channel of ≈ 4 (parameters depend on the technology) $V_{gs,p}$ is approximately 50 mV larger. For the determination of the minimum power supply current this does not have any effect for the input stage because the saturation voltage V_{dsat} for the current source in weak inversion is independent of V_{gs} . The bias circuit itself has enough headroom for this slight increase of $V_{gs,p}$. By keeping $(W/L)_p = (W/L)_n$ the die area is kept small. The following table 2.8 lists the dimension of the bias circuit.

Device	W/ μm	L/ μm	Device	W/ μm	L/ μm
M40	10	3	M44	10	3
M41	10	3	M45	10	3
M42	10	3	M46	10	3
M43	30	3			

Table 2.8: Device dimensions of the bias circuit

All devices have a gate length of 3 μm , so the noise of the current sources is kept relatively small and the current matching can be done better in the physical design than with small channel length. Due to the very simple bias structure with only two stacked devices the power supply minimum could be $V_{gs} + V_{ds}$ with the assumption that $V_{gs,p} = V_{gs,n}$.

The active load for the rail-to-rail input stage consists of the devices M7-M14. Two low-voltage current mirrors do a differential to single ended conversion and sum the currents of the n-channel and the p-channel differential input pair. M9/M10 and M11/M12, respectively, are the folded cascode transistors with a gate-voltage that adjusts V_{ds} of the mirror transistors M7/M8 and M13/M14. A minimum voltage of $2V_{gs}$ is needed for the stacked devices M7, M9, M11 and M13 and $4V_{ds}$ for M8, M10, M12 and M14 plus one V_{ds} for the floating current source of the class-AB control circuit. It is possible to insert an additional floating current source between M9 and M11 in order to minimise the power supply dependence [44]. In this design the node voltage

between M9 and M11 is adjusted by $\beta_p = \beta_n$ to $V_{DD}/2$ with the result that $V_{gs,p} = V_{gs,n} = V_{DD}/2$. The current in this branch therefore depends on the supply voltage. The dimensions of the active load devices are listed in the following table 2.9.

Device	W/ μm	L/ μm	Device	W/ μm	L/ μm
M7	10	3	M11	30	3
M8	10	3	M12	30	3
M9	10	3	M13	30	3
M10	10	3	M14	30	3

Table 2.9: Device dimensions of the load circuitry

I_d of the cascode transistors M10 and M12 of the summing circuit bias the class-AB control transistor M24/M25. One major advantage is that noise and the offset are only determined by the input stage and the summing circuit. The noise and offset contribution of the class-AB control is eliminated in that way [44]. M26 and M27 are current sources for the diode-connected devices M20/M21 and M22/M23, respectively. In the steady state the current through the floating class-AB transistors M24/M25 is divided by two into equal currents. Two translinear loops exist within the output stage consisting of M20, M30, M23 and M31. The ratio of the device sizes between the bias transistors M20 and M23 and the output transistors M30 and M31 adjust the output current. All device sizes are tabulated as follows:

Device	W/ μm	L/ μm	Device	W/ μm	L/ μm
M20	50	0.5	M21	40	0.5
M22	40	0.5	M23	12	0.5
M24	40	0.5	M25	40	0.5
M26	15	1	M27	15	1
M30	100	0.5	M31	24	0.5

Table 2.10: Device dimensions of the class-AB stage

2.3.3.1 Physical Design

In the previous sections the OPAMP architecture was discussed without considerations regarding the physical design. Important issues concerning the

analogue layout are matching of devices, noise coupling and reliability aspects. Low-voltage and low-power requirements are not directly involved. As long as the operating range of such a component as an OPAMP works at fundamental margins, layout requirements are quite critical because the higher the statistical offset the lower the ratio of signal processing range to offset. In terms of noise the SNR decreases with an increase of noise. Substrate noise is highly dependent on layout geometry [45]. The layout of the operational amplifier is shown in figure 2.26.

The layout is applicable in standard cell design because analogue components developed by the same rules can be connected at the ends of each component layout. The power supply wires have a low resistance in order to prevent voltage drops on the power supply lines. In order to reduce substrate noise the cell is entirely guard ring protected and in addition some elements have protection on a second level. Regular finger structures and centroid layout techniques are applied in avoidance of too high offsets. On the left hand side of the layout the input transistors are arranged and on the right hand side the relatively large areas are the compensation capacitors.

2.3.3.2 Measurement Results

The performance of the operational amplifier was tested in the time domain. Large and small signal behaviour can be checked by applying different test stimuli. One aim was to compare measurement results with the simulation results. A signal generator provided an input signal with a 2 kHz sine wave, as shown in figure 2.27.

A 1 M Ω resistor was inserted for bias current generation. At the output a 10 pF capacitor loaded the amplifier. For the measurement results in figure 2.28 the voltage follower configuration was used.

As can be seen in figure 2.28 the operational amplifier is able to process signals between the power supply voltage rails at the output as well as at the input. The output signal distortion comes from the limited slew rate. For small bias currents the slew rate decreases. This is expressed by equation 2.72

$$S_r = \frac{I_b}{C_c} \quad (2.72)$$

where I_b represents the bias currents I_{bp} and I_{bn} , respectively, through the input stages and C_c is the load capacitance of the input stage which is normally the compensation capacitance. C_c can be calculated from

$$f_0 = \frac{g_{mi}}{2\pi C_c} \quad (2.73)$$

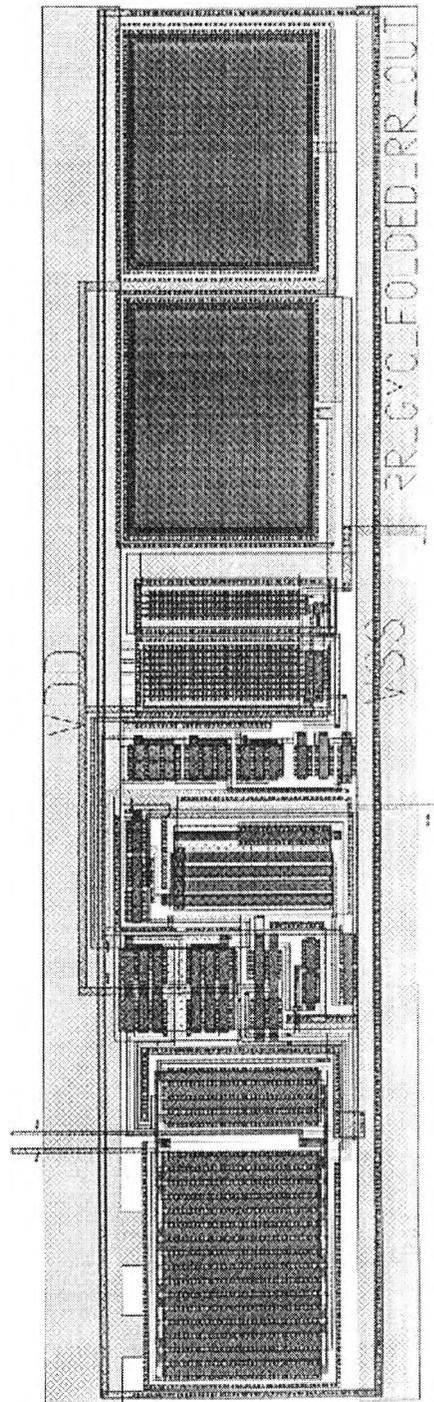


Figure 2.26: Layout Rail-to-Rail Input/Output Amplifiers

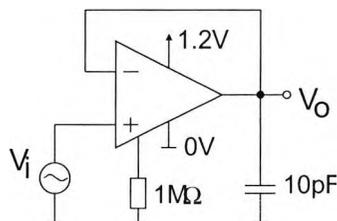


Figure 2.27: Measurement and simulation testbench of the OPAMP

where f_0 is the unity-gain frequency and g_{mi} is the input transconductance which can be either the n-channel or the p-channel input stage. The unity-gain frequency f_0 can be determined by the following bode plot of figure 2.29 which is in congruence with the measurement results.

The unity-gain frequency simulated at 1.2 V power supply voltage, 300 nA bias current and room temperature is about 20 kHz. With $g_{mi} = \frac{I_0}{nV_T}$ (Eqn. 2.17) for devices operating in weak inversion the slew rate is then

$$S_r = 2\pi f_0 n V_T \quad (2.74)$$

With $f_0=20$ kHz, $n=1.6$ and $V_T=26$ mV the slew rate is $S_r=5.2$ mV/ μ s. Comparing this result with the measurement result of figure 2.28 shows a conformability. The slew rate determined by the measurement result is around 500mV/100 μ s. This is an important result because this congruence is also expected for the optimised OPAMP.

2.3.4 OPAMP Optimization and Adaption

2.3.4.1 Power Supply Independent Bias Current

A first improvement would be a power supply independent bias circuit that generates the required bias current [24] for the OPAMP as well as for the comparator. For the low-voltage circuitries the minimum power supply voltage was evaluated as 1.2 V. For larger power supply voltages the bias current should not change in order to maintain all adjusted operating points. The bias current circuit itself has to operate stably at the minimum power supply voltage. This can only be achieved if the number of stacked devices is kept to a minimum. From the viewpoint of power consumption the bias current circuit should operate with small currents. The used circuit which is able to work at very low voltage and low currents is shown in figure 2.30 [23].

In principle the circuit consists of three parts. The basic part is the bias loop realized by the transistors M1 to M8. Two low voltage current mirrors

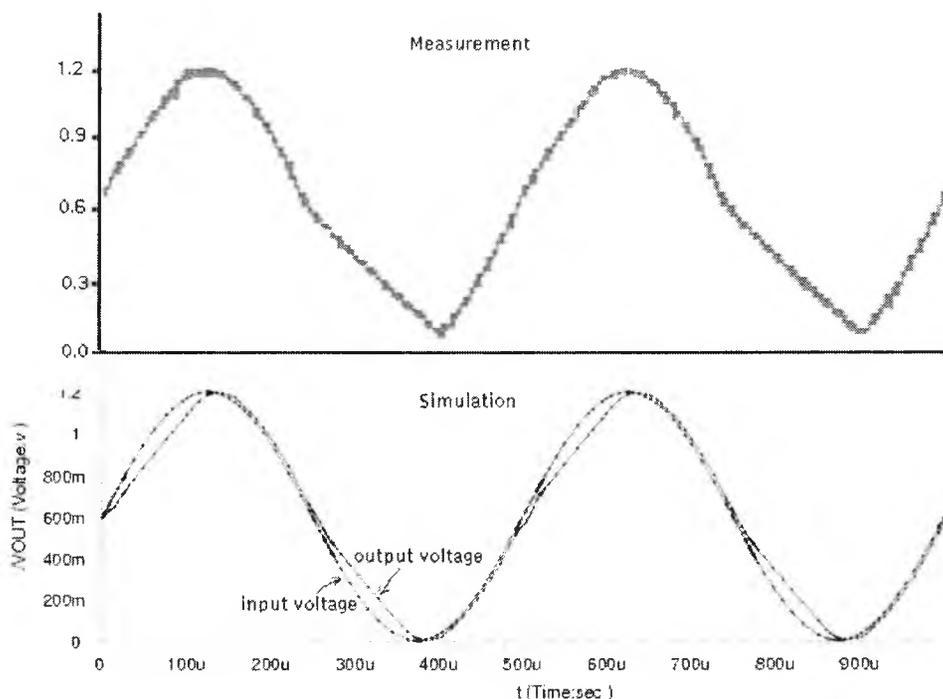


Figure 2.28: Measurement and simulation comparison

establish ideally equal currents in the branch with the odd and even numbers of the transistors. Several techniques are used to adjust the required current, based on the fact that for equal drain current, V_{gs} of M1 and M2 is also equal for equal device sizes. This solution only operates with one resistor. Other approaches insert in addition diode connected devices like diode connected MOS transistors or bipolar transistors for an improved current justification. Such techniques require higher power supply voltages.

In this approach V_{gs} of M1 is larger than V_{gs} of M2. Anticipating that the circuit operates in weak inversion, ΔV_{gs} can be calculated by

$$\Delta V_{gs} = V_{gs1} - V_{gs2} = nV_T \cdot \ln \frac{(W/L)_2}{(W/L)_1} \quad (2.75)$$

Applying Kirchoff's voltage law gives $V_{gs1} = V_{gs2} + R \cdot I_{bias}$. This equilibrium condition leads to the equation

$$I_{bias} = \frac{\Delta V_{gs}}{R} \quad (2.76)$$

Equation 2.76 is independent of the power supply voltage V_{DD} on condition that all transistors are saturated. The device sizes for the bias loop are

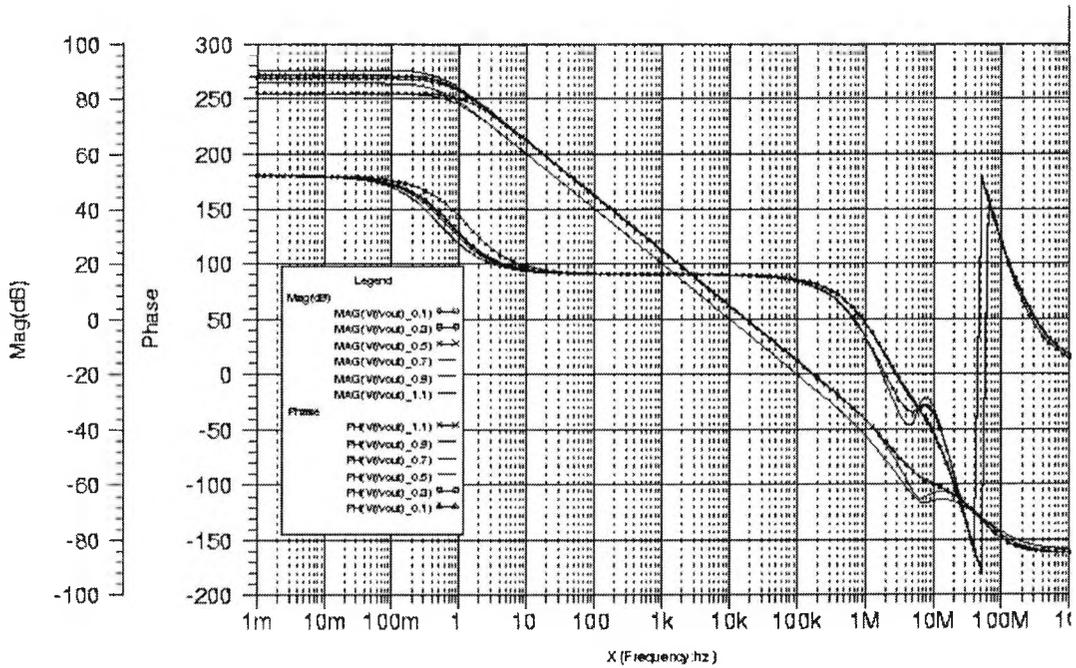


Figure 2.29: Bode plot for various common mode voltages

listed in table 2.11

For the given device dimensions and the assumption that $n=1.6$ and $V_T=26$ mV the voltage drop across R_b is about 57.7 mV. The current within the bias loop can be chosen independently of the bias current of the amplifier circuit which is supplied by this circuit. A small current of 300 nA has been adjusted by a corresponding resistor $R_b=130$ k Ω . The accuracy of handcalculation suffers from the neglected body effect which occurs in M2.

The second part of the bias circuit establishes the bias voltages for the low voltage current mirror cascode devices by the transistors M9 to M14. In

Device	$W/\mu m$	$L/\mu m$	Device	$W/\mu m$	$L/\mu m$
M1	10	2	M2	40	2
M3	10	3	M4	10	3
M5	40	3	M6	40	3
M7	40	2	M8	40	2

Table 2.11: Device dimensions bias circuit

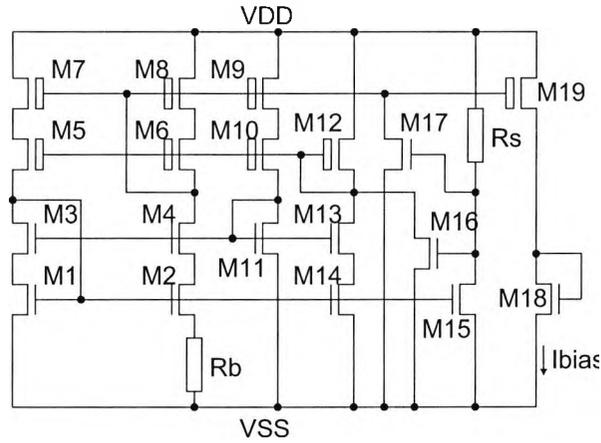


Figure 2.30: Power supply independent bias circuit

conjunction with the bias loop there is a second positive feedback loop with a small gain.

The third part is the start up circuit consisting of M15 to M17 and Rs. At start up the current in the bias loop may remain in the second of two possible steady states. In this state $I_{bias} = 0$. This is prevented by the start up circuit. Only at start up a small current is injected into the bias loop which will force the required bias current. After coming up the current injection is switched off by M15. Unfortunately the start up circuitry will consume permanent power because M15 conducts a current which is determined by Rs. A value of 500 k Ω was chosen for Rs.

With M19 the current of the bias loop is copied from this circuit. The diode connected transistor M18 can be used for replication of the current for all components in the system which need to be supplied by a stable current source.

Device	W/ μm	L/ μm	Device	W/ μm	L/ μm
M9	40	2	M10	40	3
M11	2.5	3	M12	10	3
M13	10	3	M14	10	2
M15	100	2	M16	100	1
M17	100	1	M18	25	5
M19	40	2			

Table 2.12: Device dimensions bias loop

One shortcoming of the bias circuit consists of temperature variations, because temperature effects on the resistance R_b cause changes in the bias current. For a power supply and temperature independent bias current a bandgap circuit is needed. A 1 V bandgap is proposed by Leung [46]. For evaluation of the system no temperature compensation for the bias current was needed.

2.3.4.2 Overall Topology

Basically the topology is comparable with the operational amplifier of section 2.3.3. The amplifier has a rail-to-rail input stage as well as a rail-to-rail output stage in order to satisfy the requirement for a large common mode input range and large output voltage swing. Also the active load with two low-voltage current mirrors and the control circuit for the input transconductance are similarly applied. The whole circuit is biased slightly differently, where the bias current is generated by the power supply independent bias current circuit of section 2.3.4.1. 300 nA were necessary in order to achieve a performance which is sufficient for the system requirements.

The overall amplifier is depicted in figure 2.31. Most requirements for the differential amplifier are given by the system. The fundamental requirements are a power supply voltage as low as possible and a power consumption as low as possible. The latter one is not obviously definable and enforces trade-offs in order to obtain a reasonable performance for the differential amplifier. For instance if the unity gain frequency were not be considered the differential amplifier could be biased with much less current than here proposed. Hence the performance is orientated towards comparable position measurement systems. That means in detail

- low input offset voltage
- high open loop gain
- high gain bandwidth product
- high common mode rejection
- high power supply rejection
- high temperature stability
- high slew rate
- low noise

With large input devices and also large load devices the requirement for a low input offset voltage can be realized, if layout techniques for a good matching are taken into account. This benefits in addition to a reduction of the input noise.

In low-voltage and low-power design with devices operating in weak inversion, the performance of the amplifier becomes worse. The reason is mostly the decrease of the transconductance. As given by equation 2.17, the transconductance proportional to I_d . Only some $\mu\text{A}/\text{V}$ are feasible.

The bias circuit in a low-power amplifier is an issue of importance, because each branch with current mirrors consumes power. Hence a multiple usage of bias voltages and bias currents is desired. If power consumption is not critical, the biasing could be implemented in a more sophisticated way. In this design only two branches provide the biasing for the whole circuit. With respect to low-voltage design no advanced current sources were used. They would enforce higher power supply voltages. All dimensions for bias circuit elements are summarized in table 2.13

Device	$W/\mu\text{m}$	$L/\mu\text{m}$	Device	$W/\mu\text{m}$	$L/\mu\text{m}$	Device	$W/\mu\text{m}$	$L/\mu\text{m}$
M40	40	1	M41	40	1	M42	10	1
M43	10	1	M44	10	1			

Table 2.13: Device dimensions of the bias circuitry

The differential pairs M1/M2 and M3/M4, respectively, of the n-channel and the p-channel input stages have moderate W/L ratios and they operate in the weak inversion region. The difference of the device sizes between both input stages obey the different mobilities. The ratio is for example a factor of 4. Both differential pairs have separate current sources. For the n-channel current source M6 the W/L ratio was slightly increased (compared with M42) in order to fit the current for p-channel and the n-channel input device. The device dimensions are listed in table 2.14

Device	$W/\mu\text{m}$	$L/\mu\text{m}$	Device	$W/\mu\text{m}$	$L/\mu\text{m}$	Device	$W/\mu\text{m}$	$L/\mu\text{m}$
M1	100	1.5	M2	100	1.5	M3	25	1.5
M4	25	1.5	M5	40	1	M6	11.5	1

Table 2.14: Device dimensions of the input circuitry

Within the g_m -control circuit M50 to M55 the current gain is one, because the input stage operates in weak inversion. Depending on the common

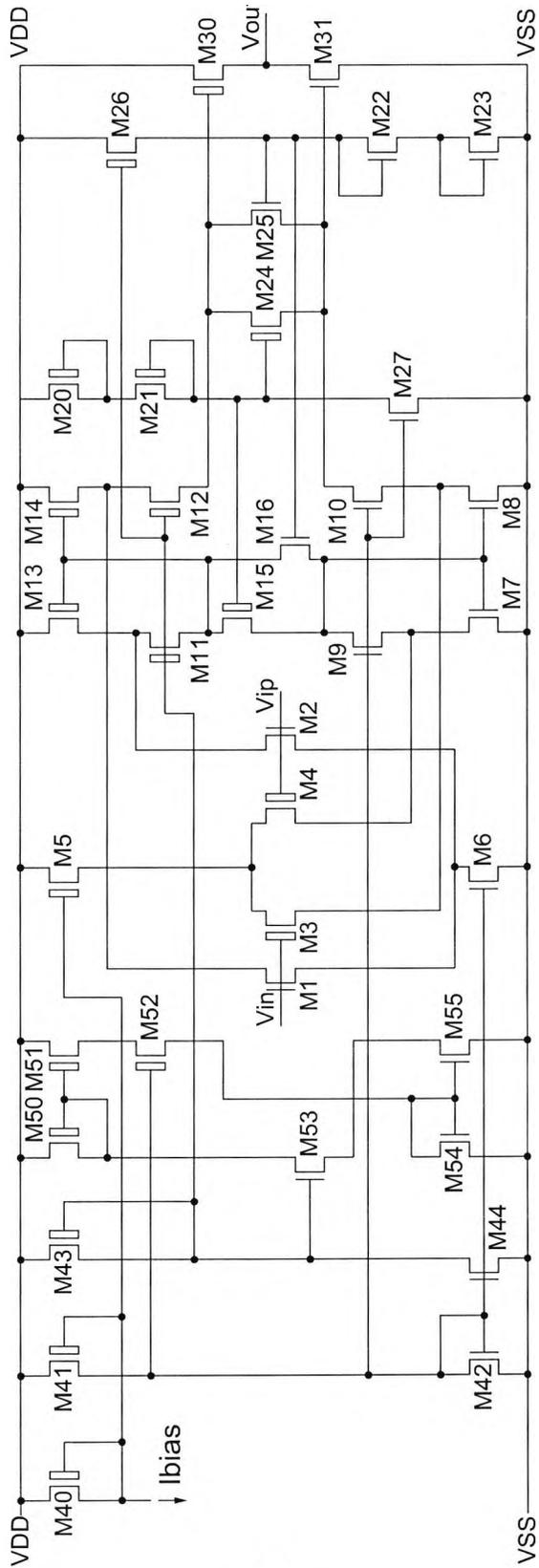


Figure 2.31: Optimised OPAMP

mode voltage this circuit either takes current from the input differential pair or adds some further current. For a constant g_m the total current I_{tot} of both differential pairs must be equal. In weak inversion the total input transconductance is given by

$$g_{m,tot,weak} = \frac{1}{2nV_T} \cdot (I_p + I_n) = \frac{I_{tot}}{2nV_T} \quad (2.77)$$

where it is assumed that the slope factor n is equal for p-channel and n-channel devices. Ideally I_p and I_n are compensated so that I_{tot} is constant. In practice an accuracy of a few percent is feasible. For the g_m control circuit the devices sizes are summarized in table 2.15

Device	W/ μm	L/ μm	Device	W/ μm	L/ μm	Device	W/ μm	L/ μm
M50	40	3	M51	40	3	M52	40	1
M53	40	1	M54	10	3	M55	10	3

Table 2.15: Device dimensions of the g_m -control circuitry

A further optimization is included in the load circuitry, where the transistors M15 and M16 establish a definite current by a floating current source. One main advantage of this approach is that such an architecture does not contribute to the offset and noise of the amplifier [44]. With the floating current source the quiescent current of the output transistors become more insensitive to variations of the power supply voltage, because M15/M16 and the floating class AB-control transistors M24/M25 are biased by the same circuit.

Regarding the quiescent current of the output transistors the circuit has been adapted to the load resistance. In this system the load resistance is very high. Hence the output does not have to drive resistances with large currents. For a power supply voltage of 1.2 V and a load resistance of 1 M Ω only 1.2 μA are necessary. Therefore the current amplification within the translinear loop of the class AB-control circuit and the output transistors can be kept small. A quiescent current of a few μA is sufficient and essential to save power consumption, particularly in low-power design. In table 2.16 all device dimensions for the load circuit, the class AB-control and the output transistor are listed.

Several other topologies of differential amplifiers would be possible. But nevertheless the developed amplifier contains circuit parts to establish low-voltage and low-power design. All efforts to reduce the power supply voltage are limited by the technology dependent threshold voltage. For low-power

Device	W/ μm	L/ μm	Device	W/ μm	L/ μm	Device	W/ μm	L/ μm
M7	10	1	M8	10	1	M9	40	1
M10	40	1	M11	40	1	M12	40	1
M13	40	1	M14	40	1	M15	40	0.5
M16	40	0.5	M20	50	0.5	M21	40	0.5
M22	40	0.5	M23	12	0.5	M24	40	0.5
M25	40	0.5	M26	15	1	M27	15	1
M30	100	0.5	M31	24	0.5			

Table 2.16: Device dimensions of the load circuitry

design the current is limited by the system performance. Furthermore large W/L ratio benefits low-voltage requirements, but on the other hand the performance suffers due to larger parasitic capacitances at low currents. In spite of an improved performance the optimised amplifier consumes less power. One of the reasons is an improved biasing of the circuit elements.

2.3.4.3 Performance Evaluation

Quite a few performance parameters exist for differential amplifiers. Apart from the absolute maximum ratings, within which a reliable usage is guaranteed, several technical parameters describe the behaviour and performance of the component. Most parameters are given in a range. This range depends on variations during processing and is therefore evaluated over a huge number of components.

The performance evaluation here is based on simulations for the most important parameters. Some worst case simulations have also been done. In conjunction with the measurement evaluations on the rudimentary components a good approximation for fabricated components is achieved.

Within the input stage the g_m -control circuit operates dependently on the common mode input voltage, as discussed in section 2.3.1.5. For evaluation, the common mode voltage was swept over the total power supply voltage range. The measured drain currents of the input transistors are taken for the calculations of both transconductances. The sum of the n-channel and the p-channel transconductance gives the total input transconductance. In figure 2.32 the simulation result is shown.

The total weak inversion input transconductance varies over the complete input common mode range of approximately 5 % which is in congruence with simulations by Hogervorst [31]. As expected, the p-channel input stage operates at low input voltages and the n-channel input stage at higher voltages.

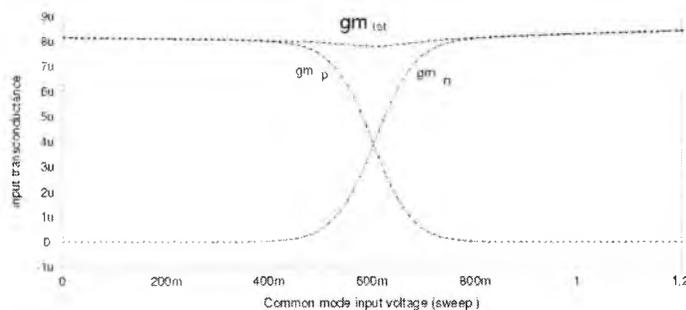


Figure 2.32: Input transconductance

One of the most important characteristic values is the unity gain frequency. It is necessary to get rid of the systematic offset during the small signal analysis. The test bench in figure 2.33 illustrates an offset free small signal simulation.

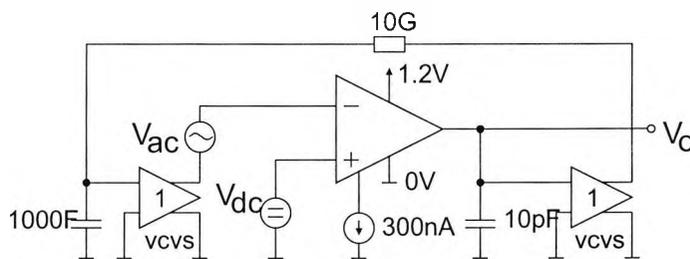


Figure 2.33: Test bench for the small signal analysis

At the output and at the input of the amplifier the voltage controlled voltage sources with a gain of 1 acts as a buffer. During the operating point analysis the amplifier is in a voltage follower configuration without an influence of the capacitor. For the small signal analysis the 1000 F capacitance is a small signal short and the very high feedback resistor realizes a very high amplification. As a result the external components do not influence the operational amplifier characteristics.

The bode diagram for different common mode input voltages is depicted in figure 2.34.

In comparison with the bode plot in figure 2.29 this amplifier has a larger open loop gain and up to 50 times higher unity gain frequency. The higher open loop gain results in a higher stability using the amplifier in a negative feedback configuration with a relative small gain. The higher unity gain frequency will also shift the closed loop bandwidth (3dB frequency) up to higher

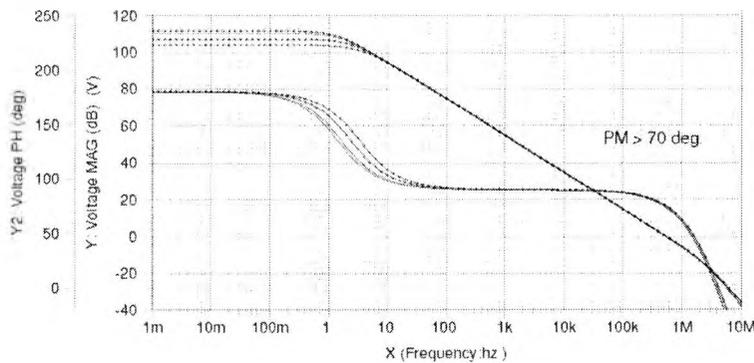


Figure 2.34: Bode diagram

frequencies. If for instance the amplification is used with an amplification of 25 as is usual in this application, the closed loop frequency is about 20 kHz which is absolutely sufficient for this sensor system. Concerning the phase margin of about $PM=70^\circ$ the amplifier obtains very small overshoots for a step response which can be also observed in the time domain simulation. For frequencies where the phase shift is 180° the amplifier has an attenuation of more than -20dB.

In the time domain the performance was evaluated with a unity gain voltage follower. The test bench is similar to the one in figure 2.27. Only the bias current generation is different. The resistor was replaced by the power supply independent bias current generator of section 2.3.4.1. A voltage step of 100 mV with a rising and falling edge of 1 ns was used in order to observe the step response at the output. Input and output voltages are shown in figure 2.35

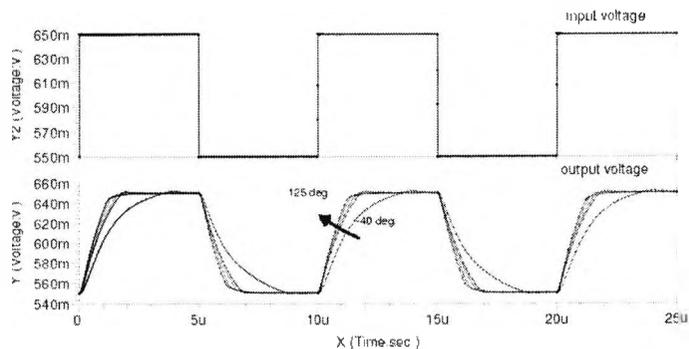


Figure 2.35: Transient response of a square waveform

With this simulation environment the slew rate of the amplifier was determined for temperatures in a range of -40°C to $+125^{\circ}\text{C}$. Obviously the slew rate increases with increasing temperatures. Equation 2.74 contains the temperature within $V_T = kT/q$. With an increase of the temperature the slew rate also increases.

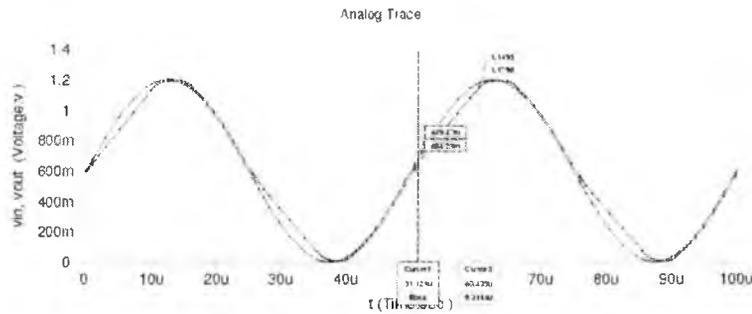


Figure 2.36: Transient response of a sine waveform

Figure 2.37 shows the test bench for the time domain simulations. It is of interest to determine the signal distortion for large output signals.

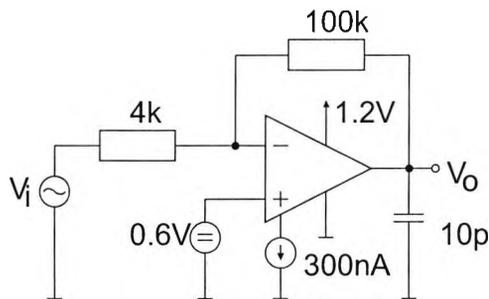


Figure 2.37: Test bench for signal distortion evaluation

For this, an amplification of 25 was adjusted. Small input signals with amplitudes in a range of 20 mV to 23.6 mV were applied with a result that the output signal gets very close to the power supply rails. The simulation results in figure 2.38 depict a FFT analysis of the output signal for a 1 kHz input signal.

As can be determined from the simulation result a slight distortion begins for very large output signals in respect of the output signal range. On the lower axis of figure 2.38 the FFT analysis result for an output signals swing of $V_{DD} - 10\text{ mV}$ and $V_{SS} + 10\text{ mV}$ is shown. The harmonic waves reach at a maximum -50dB.

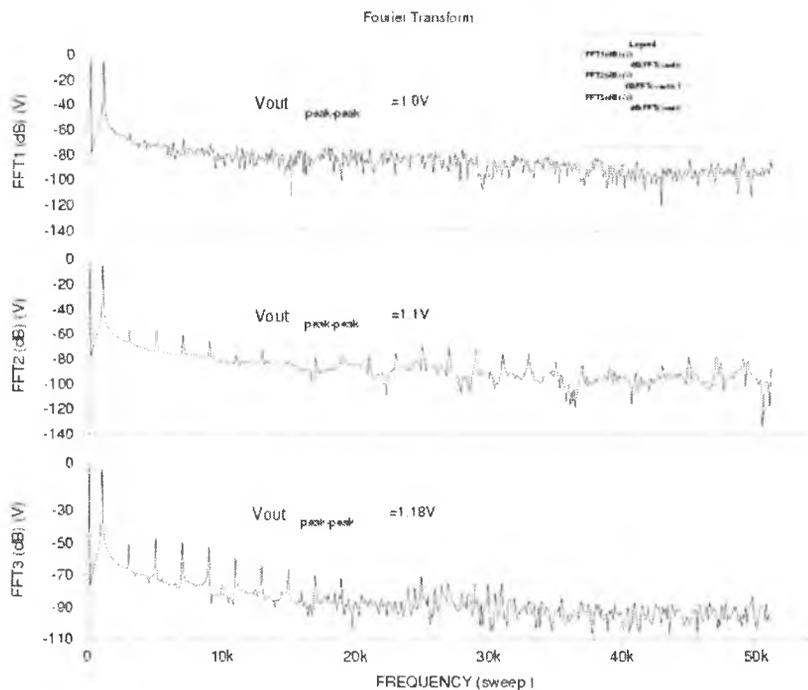


Figure 2.38: Signal distortion

The supply current for the component can change for various reasons. The dependence of the temperature was simulated. Figure 2.39 shows the simulation result.

With increasing temperatures the supply current increases. For 125°C a maximum of 13.5 μA is reached. Also the bias current of the bias current generator is depicted. The very small bias current increases from 298 nA to 394 nA. This is about 25 %. This increase in the supply current results in an increase of the total supply current of about 62 %. This is expected because the bias current is distributed into multiple branches of the amplifier.

One further reason for changes of the supply current is the common mode voltage. The currents for the differential pair over the common mode input voltage was already shown indirectly in figure 2.32. The weak inversion input transconductance is proportional to the drain current. As shown, the total current of the input stage changes by approximately 5 % and has a contribution to the overall supply current of the amplifier. The simulation result for the supply current over the common mode input voltage is shown in figure 2.40.

As a result, the supply current varies over the complete input common mode range by approximately 21 %. The maximum value of 9.3 μA is iden-

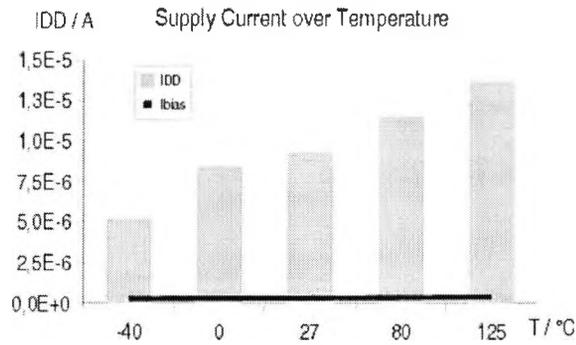


Figure 2.39: Supply current over temperature

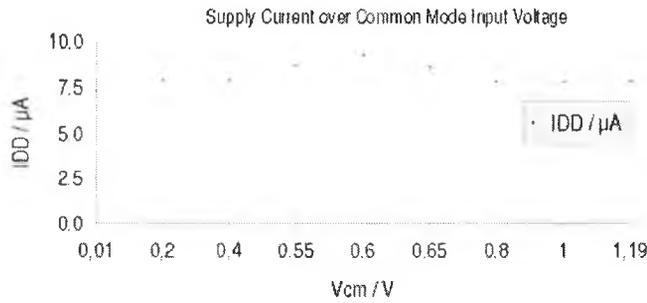


Figure 2.40: Supply current over common mode input voltage

tical to the corresponding value at 27°C of the simulation over temperature.

Several further investigations have been performed for component characterization. The results are summarized in the following table 2.17. If not otherwise noted the power supply voltage is 1.2V, the bias current 300nA, the simulation temperature 27°C and the load 10 pF in parallel to 1 MΩ.

Parameter	Symbol	Value	Unit	Conditions
Supply voltage	V_{DD}	1.2 to 3.3	V	
Supply current	I_{DD}	9.3	μA	no load
Power consumption	P_{diss}	11.2	μW	
Temperature range	T_A	-40 to 125	deg	
Systematic input offset	V_{io}	0.7	μV	
Input common mode range	$V_{i,cm}$	V_{SS} to V_{DD}	V	
High level output voltage	V_{oh}	$V_{DD}-0.03$	V	no load
Low level output voltage	V_{ol}	$V_{SS}+0.03$	V	no load
Large-signal voltage gain	A_v	95	V/mV	@0.6V
Common mode rejection	CMRR	-72	dB	$A_{cm}=22.3$
Power supply rejection	PSRR	-76	dB	@0.6V
Output resistance	R_o	480	Ω	

Table 2.17: Characteristic of the differential amplifier

2.4 Transmission Gate

A transmission gate or analogue switch is used to enable and disable analogue signals for signal processing as it is for example known from multiplexers. An obviously simple task of conducting and suspending currents can be performed by simple n-channel or p-channel devices acting as a switch. But a single transistor is limited by its threshold voltage. Similar to rail-to-rail input stages of differential inputs for amplifiers, the presence of a parallel combination of p-channel and n-channel devices make a signal processing from the negative to the positive power supply possible. A common complementary transmission gate is shown in figure 2.41.

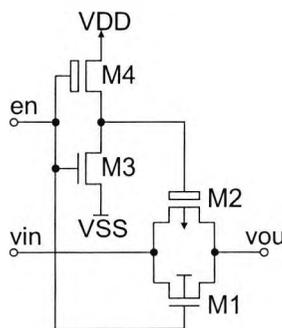


Figure 2.41: Analogue Switch

An input signal vin is transferred through M1 and M2 to the output $vout$ if the digital enable voltage en is high. The output is disabled for the case that en is low, where both devices M1 and M2 are shut off. Then the output node $vout$ becomes a very high impedance node, where no current flows into this node or comes from this node. For low-voltage operation the operating range of such a topology is limited by the threshold voltages of these devices. The minimum power supply voltage is given by

$$V_{DD,min} = V_{gs,n} + V_{gs,p} \quad (2.78)$$

The critical power supply voltage for operation is when one device is just conducting and the other is just closed - the overlapping region. In terms of voltages this means that if the input voltage is equal to $V_{gs,n}$ and the power supply voltage is so much reduced that equation 2.78 is fulfilled, then both transistors are just conducting. In this region signal distortion may be the result, caused by a nonlinear on-resistance. The resistance of an analogue switch and the influence of the reduction of the power supply voltage is depicted in figure 2.42

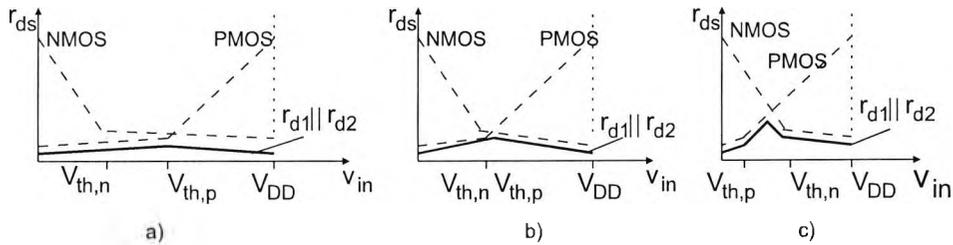


Figure 2.42: Conductance of a complementary transmission gate

Figure 2.42 a) shows the resistance $r_{d1} || r_{d2}$ that is approximately linear over the complete input range. Linearity becomes worse if the threshold voltages of M1 and M2 about (as shown in fig. b). Case c) no longer counts as a normal operation because signal distortion and the on-resistance increases. As a consequence for low-voltage design the transmission gate might be the limiting factor. This depends on several factors:

- the drain current
- the device sizes
- the body effect
- the load resistance

- the charge injection and clock feedthrough

If the load resistance is high the V_{ds} voltage drop across the transistors has a small influence. Furthermore, a high load resistance would lower the current through the transmission gate. Lower currents generate less gate-source voltages and as a result less power supply voltage is necessary for the transmission gate. Hence high impedance loads are desired. Figure 2.43 shows the output of the transmission gate if at the input a triangle voltage is applied.

Within these items conflicting requirements exist. Large device geometries would lower the resistance and V_{gs} but on the other hand the charge injection will increase. Charge injection is decreased if p-channel and n-channel devices are incorporated as a complementary switch.

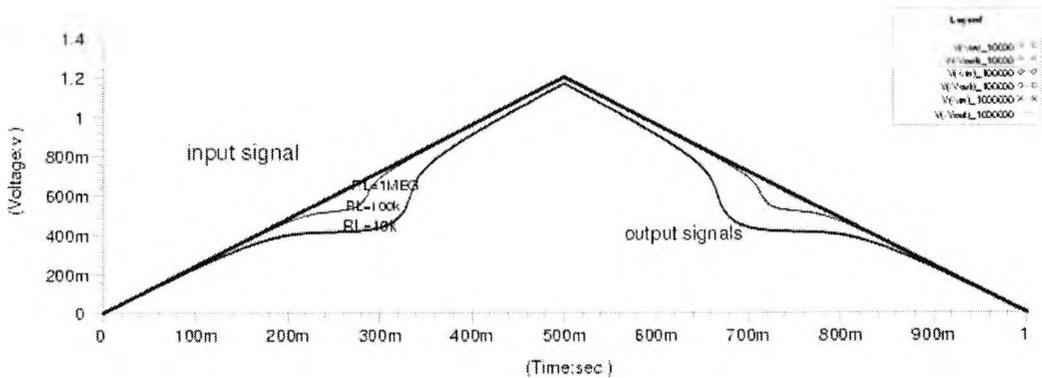


Figure 2.43: Signal distortion for low resistances

For lower resistances a higher current flows through the analogue switch. Higher currents require a higher gate-source voltage which enforces the power supply voltage to increase.

Another method by which to increase the operating range of the analogue switch is to bias one of the transistors in a different way. This depends on the type of the substrate. For a N-Well technology the bulk of the p-channel transistor can either be biased by a voltage or the source and the bulk terminal can be shorted. With the first method the threshold voltage can be reduced, the second one prevents the body effect that occurs for the analogue switch. The low-voltage implementation is sufficient to prevent the body effect. The improved circuit is shown in figure 2.44.

Using a combination of the architectures prevents the body effect and in addition a high impedance load will allow a proper operation of the analogue switch at the same operating voltage as the OPAMP and comparator. The

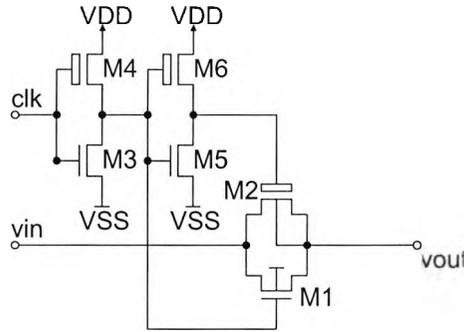


Figure 2.44: Complementary transmission gate with bulk biased PMOS

simulation result which shows the difference of the input and output voltage is depicted in figure 2.45 .

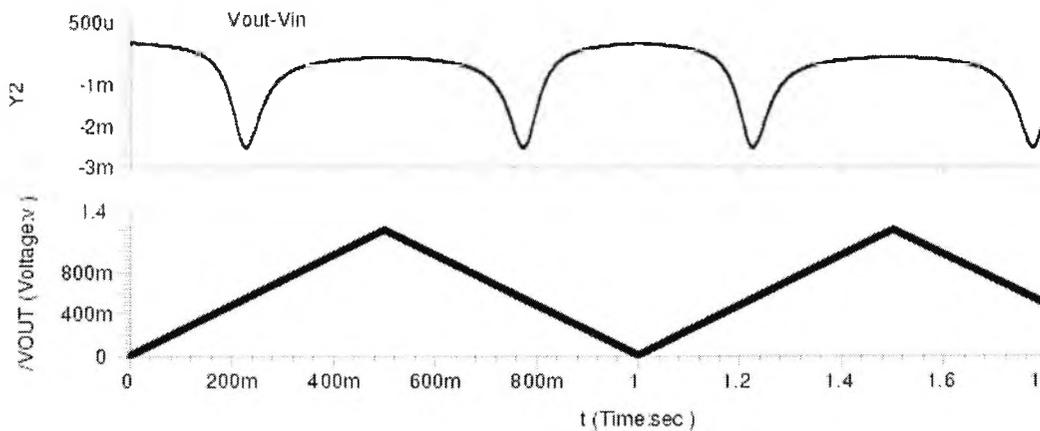


Figure 2.45: Simulation result of the improved switch

This simulation result shows that the voltage drop across changes over the complete common mode input and output range by about 2.5 mV. This is an acceptable value but causes a small signal distortion.

2.5 Digital Cells

Some tasks of signal processing must be done by digital computation. In this work digital cells are used for decoding some states of the comparators. The system requirements are not influenced by the digital part. For a proper operation of the digital part $V_{DD,min}$ must be larger than the largest V_{th} of

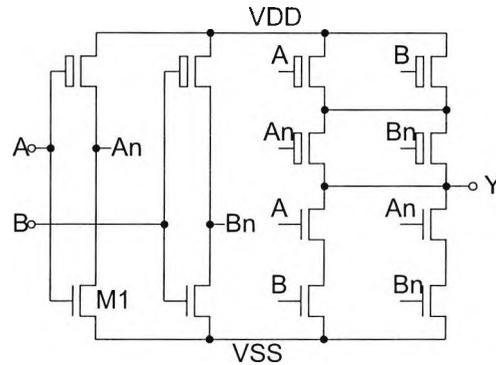


Figure 2.46: Exclusiv OR gate

the n-channel or the p-channel, respectively, in order to guarantee the transistors are fully switched on. Working at the threshold margin would result in a higher resistance compared with devices that have a higher overdrive voltage. The resistance in conjunction with the load capacitance determines the maximum signal processing speed.

For the realization of some digital parts, gates as AND2, AND3, OR2, OR3, Inverter, Buffer and XOR have been used. As an example, a XOR gate with four stacked transistors has been investigated for low-voltage operation. The schematic of the circuit is shown in figure 2.46.

Two output states are possible for a gate. In the case of zero, one of the branches from Y to VSS has a very low impedance. Both of the two transistor of one branch have gate-source voltages, which must be larger than the threshold voltage V_{th} . Subthreshold operation for digital circuits is also possible but would also lower the signal processing speed significantly. In this work subthreshold voltages for digital elements are not feasible and not necessary. If strong inversion operation is assumed the minimum power supply voltage for the digital circuit $V_{DD,min}$ is given by

$$V_{DD,min} = V_{th} \quad (2.79)$$

where V_{th} could be either the threshold voltage of the p-channel or of the n-channel transistor, depending on which is larger. Each of the stacked transistors must be driven by gate voltages larger than V_{th} . There is no increase of the gate voltage, because the highest transistor of the n-channel branch pushes the lower ones out of saturation. No drain-source voltage will occur for lower transistors. Therefore all transistors have the same gate-source voltage which is $V_{DD} - V_{SS}$.

Power supply voltages which are close to the threshold voltage slower

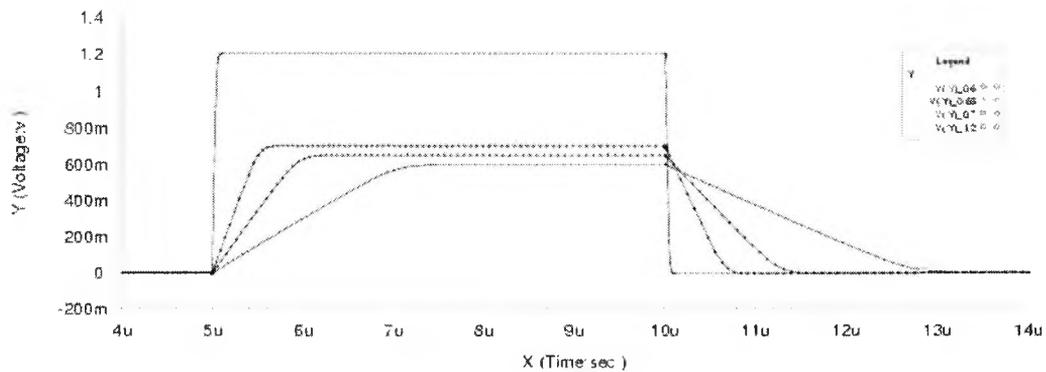


Figure 2.47: Signal processing speed as a function of V_{DD}

the signal processing speed. Figure 2.47 shows this dependence for an input signal with 100 kHz clock rate.

As figure 2.47 shows, the rising and falling time of the edges increase with lower voltages and they would increase further for subthreshold operation. For a power supply voltage of 1.2 V the time of the rising and falling edge is about 46 ns. This is absolutely sufficient for the digital signal processing of this circuit.

As a result, the power supply voltage for the system is limited by the analogue components.

Chapter 3

System Architecture

3.1 Sensor Input Interface

3.1.1 Sensor Element and Gauge

A wide variety of sensors are used for position measurement systems. Many sensors use the same idea to generate position information. Basically this idea deals with two or more phase shifted signals, where the phase shift contains the direction information and the signals themselves the position information. The position information for low resolutions can be simply generated with a couple of comparators detecting some signal points. A higher resolution can be achieved with much more effort in signal processing, which is very often the case for position information below 1 mm.

In this chapter a new method for increasing the resolution will be presented. This method can be applied for all sensors which generate two sine wave output signals that are shifted by 90 degrees. In particular magneto resistive sensors are well suited for this application.

Anisotropic Magneto Resistive (AMR) sensors used in position measurement systems are stimulated by a magnetic gauge. Only in conjunction with a magnetic gauge does the sensor deliver the required signals if the sensor element and gauge are fitted with respect to one magnetic pole. That means that some geometrical dimensions of the sensor and the gauge have to be as identical as possible. Two Wheatstone bridges are placed on the sensor element chip. They have a fixed shift of $P/4$ (90°) relative to P of one magnet pole (360°) as depicted in figure 3.1.

Magneto resistive sensors are commonly constructed with only two phase shifted sine signals as is also common for other sensor elements - for instance optical sensors. Typically, the phase shift can be either $+90^\circ$ or -90° . This enables the detection of the movement direction to be deduced from the

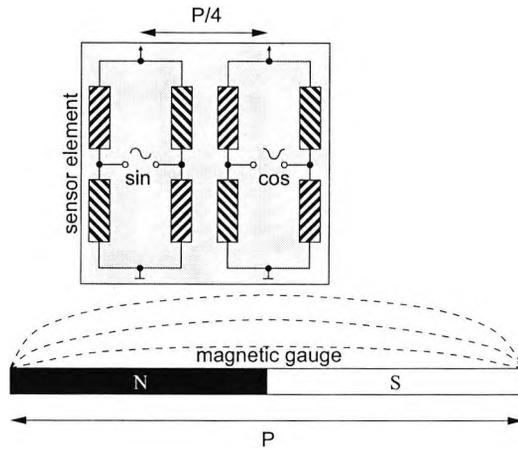


Figure 3.1: Wheatstone sensor bridges with a gauge

phase relation. The ideal output signals of such a magneto resistive sensor are therefore sine and cosine waveforms. They have an ideal DC level of half of the supply voltage (Eq. 3.1) and an amplitude that is in the range of some mV per V of the power supply voltage (Eq. 3.2), if the sensor is driven by a voltage and not by a current .

$$V_{DCs} = V_{DD}/2 \quad (3.1)$$

$$5mV/V \leq V_{ACs} \leq 15mV/V \quad (3.2)$$

The DC voltage level as well as the amplitude of the sensor element is scaled linearly by the power supply voltages, which can be derived from the equations 3.1 and 3.2. Both are scaled in a linear fashion. That means in respect of the system architecture, that the sensor supply voltage does not limit the system requirements. The smaller the power supply voltage the smaller the amplitude and DC level. In the following figure 3.2 the difference output signals of the sensor element (both Wheatstone bridges) are shown.

On the one hand advantages of this sensor element are that

- the sensor operates at low voltages,
- the offset is scaled down linearly with decreasing power supply voltage,
- the power consumption is scaled down linearly with decreasing power supply voltage

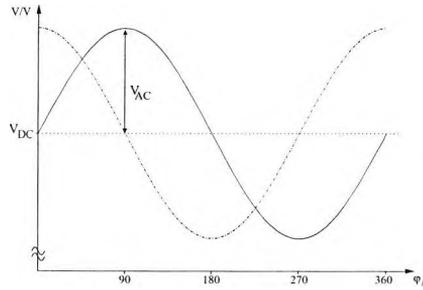


Figure 3.2: Sensor element difference output signal

- the frequency bandwidth is very high and without any influence on the system and
- available sensor elements with high resistances benefit low power systems, due to very low power consumption

On the other hand some negative effects may occur due to the sensor element and gauge mismatch in respect of their dimensions. The sensor element geometries are fixed whereas the magnetic gauge device has scattering. This is an elementary point for linearizing the signal and can lead to errors of position measurement due to signal distortion. Further undesirable effects due to disturbing magnetic fields can occur, because conventional sensor elements cannot distinguish between a magnetic signal field and a disturbing field. But this is not an issue of this section of the work. This is considered within chapter 4 of the sensor model. The influence that this effect has on the system will be investigated, in order to evaluate the efficiency of the system.

In summary the magneto resistive sensor generates the required signals for position measurement without imposing any limitations on the system architecture. Therefore it can be considered as an excellent solution for all two phase sensor elements for position measurement.

3.1.2 Sensor Noise

The output signal of a magneto resistive sensors may not be considered constant if a fixed magnetic field biases the sensor. As is natural for resistors, noise also occurs in magneto resistive Wheatstone bridges. The margin of resolution of a magnetic field is determined by [6]

$$Q = \frac{v_n \cdot \mu_{m0}}{s \cdot V_{dd} \cdot \sqrt{\Delta f}} \quad (3.3)$$

where v_n is the noise voltage, μ_{m0} is the magnetic field constant, s is the standardised sensitivity of the sensor, V_{dd} is the power supply voltage and Δf is the bandwidth. From the system viewpoint this is a surprising result, because the resolution increases with smaller power supply voltages. For low voltage applications such sensors are therefore well suited.

Above several hundred Hertz the white noise (also called thermal, Johnson or Nyquist noise called) dominates. The rms value of the noise voltage is given by

$$\overline{v_{n,sensor}^2} = 4kT \cdot R \cdot \Delta f \quad (3.4)$$

where k is Boltzmann's constant, T the absolute temperature, R the resistance and Δf the bandwidth. Sensor elements with a lower resistance generate less noise but for low power applications a resistance as high as possible is desired. Hence a compromise must be found in terms of the total input noise voltage at the interface of the sensor element and the input amplifier of the electronic circuit. Neither the power consumption of the sensor nor the sensor noise should dominate.

Apart from the white noise of the sensor element a frequency dependent noise source exists for magneto resistive sensor elements. This has been investigated by [38] [39] resulting in two different theories. In order to prevent a deeper discussion of sensor specific details only the white noise of the sensor element is taken into account.

3.1.3 Signal Amplification

At the interface between the sensor element and the electronic circuit the load resistance caused by the input amplifier should be negligible. Instrumentation amplifiers provide an extremely high input impedance. Two types of instrumentation amplifier are commonly used. One type of implementation consists of two differential amplifiers and the second type consists of three differential amplifiers. The latter one was used for this sensor system. Figure 3.3 shows the schematic.

Compared with the dual op-amp type this triple op-amp instrumentation amplifier needs one more amplifier and in addition more resistors. In terms of chip area and power consumption these are two significant drawbacks. But the advantage of the triple op-amp case is the symmetric signal processing. Differential amplifiers with a low bandwidth induce errors because of the phase shift for relatively low frequencies. With the symmetric triple-op-amp instrumentation amplifier the phase shift will not have any effect on the signal processing. Furthermore this instrumentation amplifier usually has a higher

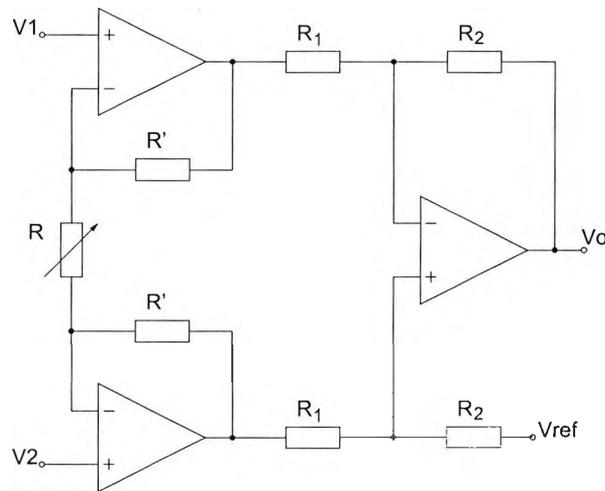


Figure 3.3: Instrumental amplifier

CMRR performance over a broader frequency range [57].

The inputs of the instrumentation amplifier are connected to the difference output of the Wheatstone bridge and do not load the sensor element. The terminal V_{ref} is typically connected to $V_{DD}/2$ if unipolar power supply voltage is applied. The generation of $V_{DD}/2$ is done by a voltage divider. In order to prevent an influence of this voltage divider, a unity-gain amplifier acts as a resistance transformer between the voltage divider and node V_{ref} .

Instrumentation amplifiers as shown in figure 3.3 have two gain stages. The product of the gains of both stages gives the overall gain A_v of

$$A_v = \left(1 + \frac{2R'}{R}\right) \cdot \frac{R_2}{R_1} \quad (3.5)$$

The two stage architecture also benefits the bandwidth of the system, if the gain is distributed on both stages. Otherwise the closed loop frequency is determined by the stage with the highest amplification. For this system an amplification of 25 was necessary. Each stage has therefore an amplification of $\sqrt{A_v}=5$. This results in $R_2 = 5R_1$ and $R = 1/4R'$. These are reasonable values with respect to matching considerations in the layout.

3.2 Signal Conditioning Methodology

3.2.1 Resolution and Resolution Enhancement

As introduced in section 3.1.1 the output of the sensor is a sine and a cosine signal. What kind of information concerning the position do these signals include, while moving the sensor along the gauge (Fig. 3.2)? One period P is a fixed length related to the sensor and gauge geometry. The minimum resolution Ψ_{min} is given by

$$\Psi_{min} = \frac{P}{4} \quad (3.6)$$

For instance, if the period is 1 mm then the resolution is $250\mu m$, which is very unprecise for most applications. The reason for the minimum resolution being four times higher, is that the sensor delivers two signals within one period. If these two signals are converted into the digital domain, then the sine as well as the cosine become a digital signal with the same frequency compared with the analogue counterpart. Within one period of the digitized sine and cosine each signal has two edges and both together four, as shown in figure 3.4.

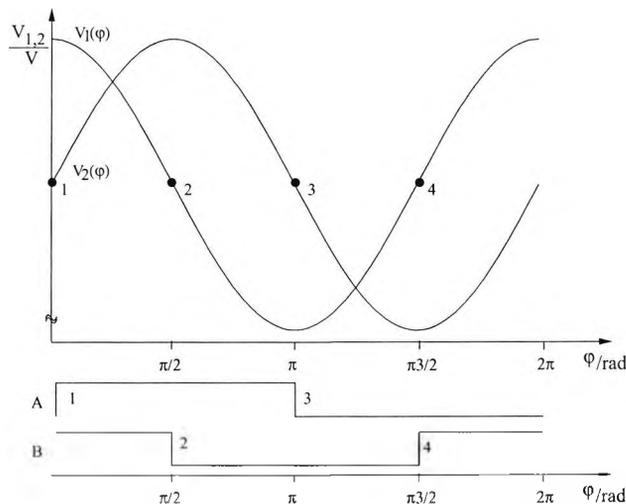


Figure 3.4: Minimum resolution of the sensor signal

Many position measurement systems [13, 14] operate with this resolution (Eq. 3.6). In order to increase the resolution by digitizing the analogue signal with the above described method, the period has to become smaller, but several problems occur if the period becomes significantly smaller. For

instance if the geometry shrinks from 1 mm to 100 μm , then the structures are very small and it is very often impossible to fabricate sensor elements with such small geometries.

Nevertheless requirements for higher resolutions are given as it is usual in production of machines parts or angle measurements in motors. As a result, the resolution has to increase with other methods. The increase of resolution can be done by interpolation of the analogue input signal. In figure 3.5 this principle is shown.

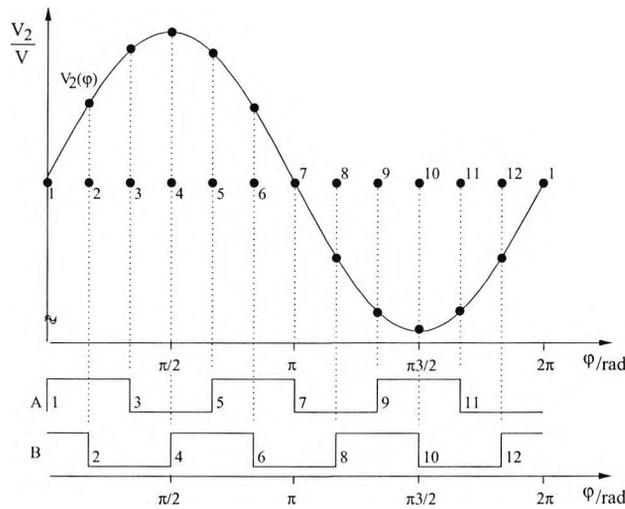


Figure 3.5: Increased resolution

On the electronic level some components have to be provided to do analogue signal processing and interpolation. In nearly all topologies components like operational amplifiers and comparators are needed. Hence these components are developed as basic cells (Chapter 2).

Traditional interpolation circuits were not designed with regard to low voltage and low power aspects. In order to reach the aim of this thesis, the circuit must be improved also on a system level. The major idea is to save energy on a component or element level and to save components on a system level, which reduces the total power consumption. In the next section 3.2.2 the concept is introduced, which significantly reduces the number of components.

3.2.2 Folding A/D conversion concept

3.2.2.1 Dynamic Range of Flash Converters

Most electronic system architectures include a conversion of the analogue input signal from the analogue to the digital domain. Where the ADC is placed in the system varies with its application and depends on the analogue input signal. It can be placed directly at the analogue sensor interface or after an analogue signal conditioning circuit (fig. 3.6).

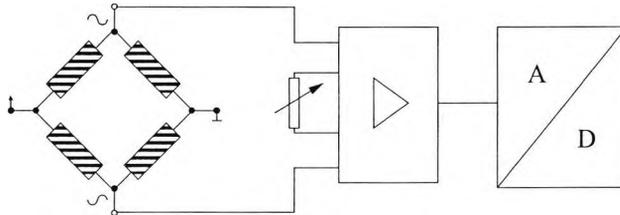


Figure 3.6: Conventional sensor interface

The analogue conditioning circuit is in most cases only an amplifier. Basically the reason is to enlarge dynamic range DR. This is also an important point for ADC working in a low voltage environment. Naturally the dynamic range is reduced because of a smaller possible signal amplitude, which is limited to the power supply voltages. The dynamic range is given by

$$DR = 20 \log \frac{S}{N}, \quad (3.7)$$

where S is the rms amplitude of the largest signal and N the rms amplitude of the smallest signal - the noise. The quantization noise of the ADC must also be considered. For a perfect, noiseless ADC N is $1/\sqrt{12}$ LSB rms. As a result, the DR can be maximized if the S is maximized. Ideally the signal ranges from the negative to the positive reference voltage, which is in the best case the power supply range. S depends on the resolution which can be expressed as $2^n/(2 \cdot \sqrt{2}) \cdot \text{LSB}$ rms. Then the dynamic range is given by

$$DR = n \cdot 6.02 \text{ dB} + 1.76 \text{ dB}. \quad (3.8)$$

Full flash converters [20] are used in applications with high input frequencies and for continuous time applications without sample and hold circuitries [23, 24]. The simple full flash converter architecture contains 2^n numbers of comparators in parallel as depicted in figure 3.7. Applications with high resolution requirements therefore need a large number of components for

the full flash ADC. Each additional bit entails approximately a doubling of components, of power dissipation and chip area [25].

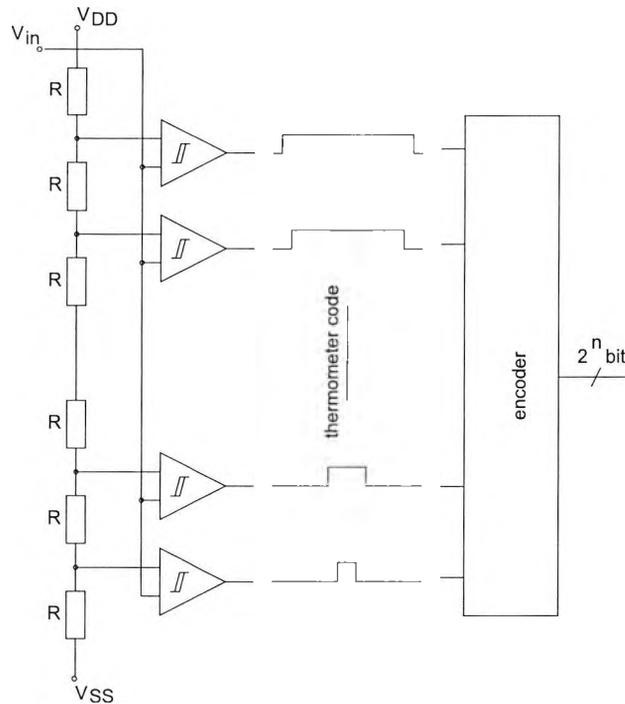


Figure 3.7: Conventional flash ADC

If this architecture is used in sensor applications this method suffers from a fixed dynamic range. The signal amplitude of many sensor elements is not fixed due to several influences like unstabilized power supply voltages or variations of the sensor parameters. Further influences concerning the signal amplitude may be the sensor displacement or the sensor environment. Then the rms amplitude S does not fit to the dynamic range. This is also the case for magneto resistive sensors. One solution may be a gain control circuit that fixes the input amplitude to the maximum of the conversion range, then equation 3.7 is fulfilled. In real applications this is an ideal case. Therefore it is desired to be independent of loss in the dynamic range due to loss of signal amplitude. Another practical solution may be to increase the resolution n (eq. 3.8), but for flash converters this is not suitable, particularly if the flash converters are to be improved with regard to power consumption.

3.2.2.2 Dynamic Related Reference for Flash Converters

As discussed in section 3.2.1 one property of such sensor outputs as they are for instance provided by a magneto resistive sensor, is that the sine and cosine signals can be mathematically divided and as a result the signal processing becomes independent of the signal amplitude [10]. Based on this special case for these types of sensor element the input architecture of the flash ADC can be changed as depicted in figure 3.8

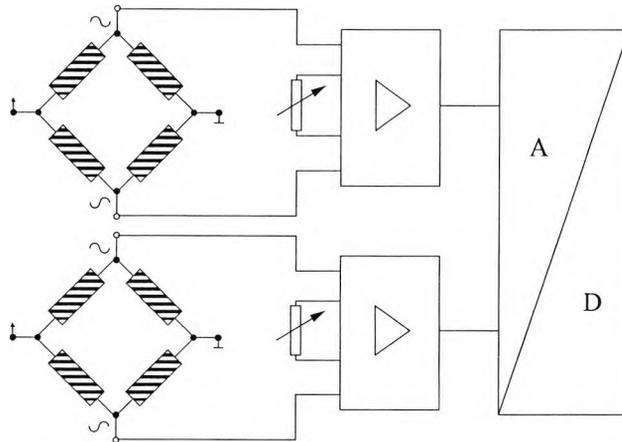


Figure 3.8: Concurrent ADC signal processing of sine and cosine

A single ADC (fig.3.8) processes both sensor signals concurrently. This is different from most types of signal processing that use separate ADCs for each channel (sine and cosine). In order to satisfy low power aspects it is more efficient to process signals with a single ADC. As proposed by [10] the two phase shifted input signal voltages are added with two resistors as shown in figure 3.9. The values of the resistors R_1 to R_n are weighted in such a way that a special phase of the input signal is selected. This has been done for several phases. With analogue comparators in conjunction with the resistors the input signals are converted into the digital domain.

With this kind of topology the signals themselves determine the dynamic range. There is no loss due to input signals that are smaller than the dynamic range of equation 3.8. The major differences are that the resistor string is not referred to ground. The inputs of the resistor string are driven by two dynamic signals.

Consider the resistors of figure 3.9. The load resistance R_L of the two voltage sources V_1 and V_2 is given by

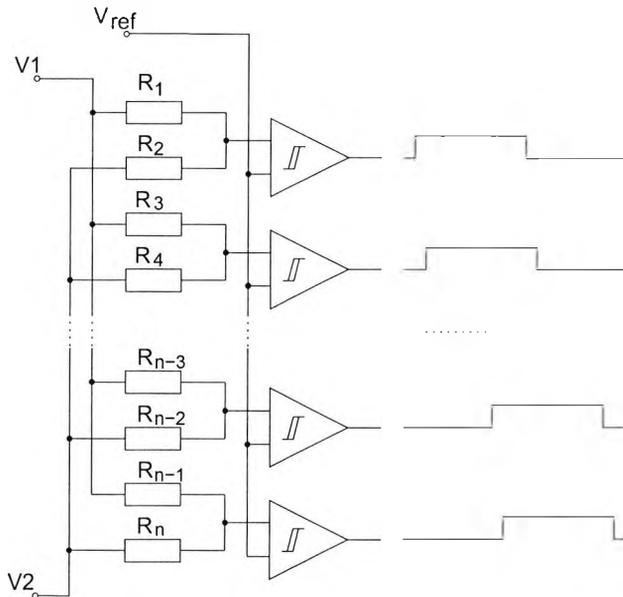


Figure 3.9: Concurrent ADC signal processing of sine and cosine [10]

$$R_L = (R_1 + R_2) \parallel (R_3 + R_4) \parallel \dots \parallel (R_{n-3} + R_{n-2}) \parallel (R_{n-1} + R_n), \quad (3.9)$$

if the source resistances are neglected. When increasing the resolution of this flash converter the load decreases. Taking low power aspects into account this topology is not suitable because the current increases with higher resolutions. For this architecture the resistors must be chosen to be very large. This is also necessary in order to reduce matching errors of the resistors.

Due to these above mentioned shortcomings the resistor arrangement of the flash converter should be changed. The proposed architecture is new.

Instead of putting the resistors in parallel (see Eq. 3.9) the resistors are arranged in series as commonly done for flash converters. In this architecture the terminals at the end of the resistor string are connected to the input signals V_{f1} and V_{f2} . Finally the resistor string is a high ohmic load for both voltage sources. The architecture is depicted in figure 3.10.

If the flash converter of figure 3.9 is compared with this ADC the same advantage of the dynamic range can be observed which is determined by the input signal itself. The output voltages can be expressed by

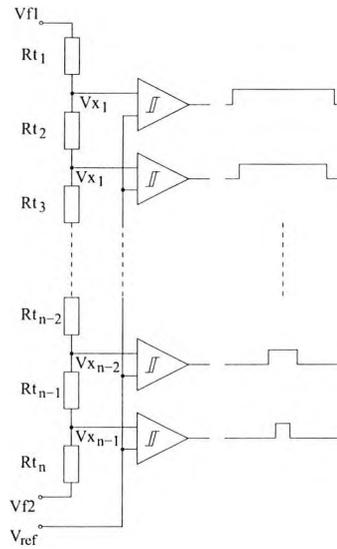


Figure 3.10: Flash ADC with symmetrical input signals

$$Vx_i = \frac{\sum_{k=1}^i R_k}{\sum_{k=1}^n R_k} (V_{f1} - V_{f2}) + V_{f2} \quad \text{for } i = 0, 1, 2 \dots n. \quad (3.10)$$

For conventional converters it is typical to express the range of equation 3.10 up to 2^n . The resolution needs not necessarily be based on digital values. In many cases of sensor signal processing the quantization of the ADC is much higher than needed and after digital computation, reduced to suitable ranges. Hence, the ADC can be designed for special resolutions or quantization ranges, for instance 100. With this approach the goal of minimizing the power consumption is reached in the best possible way. Consequently the quantization has to be reduced in a most essential range. Therefore the range of equation 3.10 has an upper limit of n and not 2^n .

In order to analyse the node voltage, it is possible to simplify the resistor ladder with a model. This model is valid for both described ADC architectures, where the voltage drop at each comparator V_x can be modeled as depicted in figure 3.11, where R_1 is the sum of all resistors between the terminal V_{f1} and V_x and R_2 is given by the sum of the resistors between V_x and V_{f2} .

Applying Kirchoff's voltage law on this circuit (fig. 3.11) yields equation 3.11.

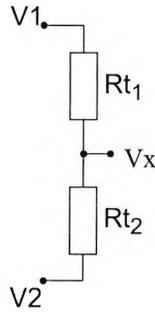


Figure 3.11: Model for the resistor string taps

$$V_x = \frac{R_2}{R_1 + R_2} V_{f1} + \left(1 - \frac{R_2}{R_1 + R_2}\right) V_{f2} \quad (3.11)$$

This equation is the base for the further development of the resistor string (sec. 3.2.2.3). As a result the voltage $V_x = f(V_{f1}, V_{f2}, R_1, R_2)$, where the voltages V_{f1} and V_{f2} are special waveform signals from the amplified sensor output.

As a consequence of driving the ADC with signal voltages across the resistor ladder, the frequency behaviour of such a flash converter topology is different. The small signal model is depicted in figure 3.12.

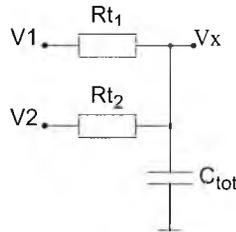


Figure 3.12: Frequency model for the resistor string

The total resistance seen at node V_x is $R_{tot} = Rt_1 \parallel Rt_2$, where the total resistance is different at each node. Rt_1 and Rt_2 are the resistances seen at the taps, whereas the total capacitance is fixed, because the total resistance is given by $C_{tot} = Ct_1 \parallel Ct_2 \parallel C_{i_{comp}} = Ct_1 + Ct_2 + C_{i_{comp}}$. Indeed the capacitances at the taps Ct_1 and Ct_2 changes but the sum of both is always the same and also the input capacitance of the comparator $C_{i_{comp}}$ is always determined by one comparator. Depending on the resolution or rephrased the number of taps the time constant at each node can change in a range of 10

to 100. Assuming a technology dependent resistance of $R_{square} = 2k\Omega/\mu m^2$ and $R_{tot} = R_{square} \cdot L/W$, where L is the length and W is the width of the resistor and R_{tot} should be $100k\Omega$ and W is $5 \mu m$, then the resulting resistor length is $250\mu m$. For simplicity the resolution is 100 and low voltage and low power aspects therefore the smallest resistor is $1k\Omega$ and the largest resistor is $50k\Omega || 50k\Omega = 25k\Omega$. Furthermore the parasitic capacitances of the resistor should be for instance $C_{square} = 0.1fF/\mu m^2$. Then $Ct_1 + Ct_2$ is $0.125pF$. If we add a parasitic input capacitance of the comparator of approximately $0.5pF$ we can determine f_{-3dB} in a range of ≈ 10 MHz to 250 MHz. In spite of this undesired effect the limitation is given by the previous signal processing components, as discussed for the low power and low voltage circuit components in section 2. This low pass filter characteristic does not have any influence on the signal processing if the technology parameters are in the range as assumed. If the resistor area is much larger as well as the input capacitance of the comparator and the technology parameters are worse, there could be an influence.

3.2.2.3 Input Signal Folding

Several folding techniques are known in electronic circuit design. Some of them have diffused significantly like the folding cascode concept of operational amplifiers. Also for A/D converter design folding techniques are known. In 1979 the full-parallel flash converter principle [20] was improved by a technique that separates the signal processing into two parts - a coarse and a fine parallel A/D conversion, where the coarse signal is subtracted from the input signal. This technique is called "Two-step folding A/D converter" and is in general the origin of methods that are able to reduce the number of comparators within flash converters. The basic idea is to save components with folding techniques, as proposed by van de Grift and van de Plasche in 1984 [22]. They reported positive results for power dissipation reduction while achieving an excellent performance compared with full-parallel flash converters without folding techniques [25]. Several papers followed with improvements, for instance, interpolating techniques or multiple folding [25], [26], [27], [28], [29], [30]. Figure 3.13 demonstrates the folding principle.

With this technique a transformation of the input is achieved in order to split the input signal into a coarse and a fine signal. Both the coarse converter and the fine converter form the digital output signal. At the input the coarse converter is active over the total voltage range of the ADC and the fine converter uses only a part of the total voltage range several times. This is shown in figure 3.14.

The same idea of signal folding is pursued in this work. As discussed in

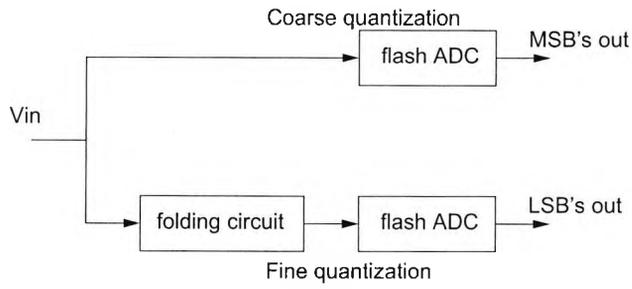


Figure 3.13: Folding concept for ADC

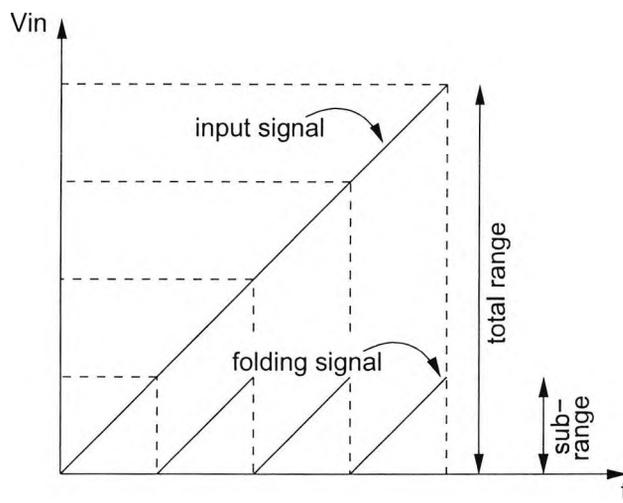


Figure 3.14: Folding principle

section 3.2.2.2 the ADC structure distinguishes itself concerning of the concurrent signal processing of two input signals. Hence, the published folding techniques do not fit. For instance, if the two phase shifted sine formed signal (fig. 3.2) are applied at the two terminals of the resistor ladder (fig. 3.10) the voltage drop across the resistor ladder becomes zero for the condition $V_{f1} = V_{f2}$. This must be prevented by a preceding signal processing.

Consider figure 3.15 in regard to signal symmetry of the input signals. The smallest possible symmetry is 45° or $\pi/4$ within one complete period.

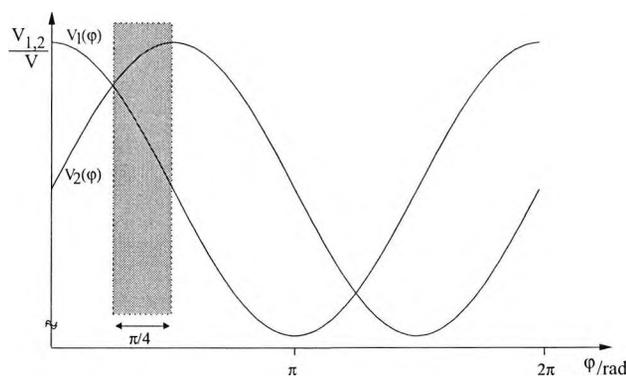


Figure 3.15: Principle of Signal Symmetry

In order to perform a signal processing regarding the smallest possible signal symmetry, the input signals must be also represented by their inverted counterparts. Then the symmetry is available as depicted in figure 3.16.

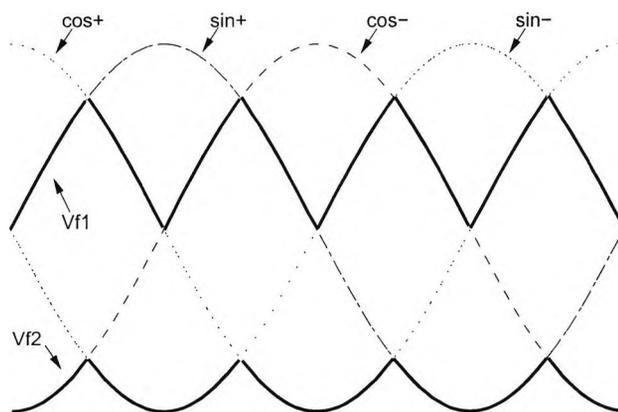


Figure 3.16: Signal transformation

The bold lines in figure 3.16 are the desired signals for signal processing.

The shortcoming mentioned above, of voltage differences of zero across the resistor ladder is bypassed if the upper bold signal waveform is applied at the first terminal of the resistor ladder and the lower bold signal waveform at the second terminal.

A signal processing unit that transforms the narrow signals of figure 3.16 into the bold ones is advantageous in the same way as the signal folding of figure 3.14. The number of comparators in the sequencing AD converter is reduced. With this kind of signal folding the conversion range is reduced by a factor of $2^3 = 8$, because the symmetry is an eighth of the period. If the argument is referred to the conversion range of one sine between the minimum and the maximum value the improvement is by a factor of 4. If two ADC are used, the benefit of such folding architecture is 8 again. The topology of the signal folding unit is shown in figure 3.17.

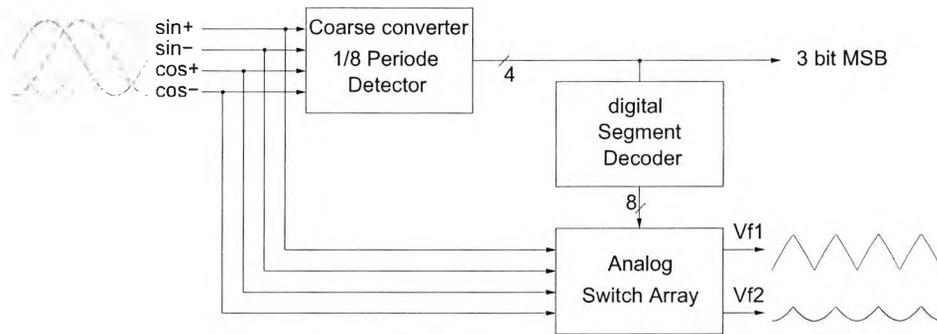


Figure 3.17: Signal folding architecture

The coarse converter in figure 3.17 includes 4 comparators. Of the 16 possible states of the 4 bits only 8 states occur, due to the fixed phase relations of the four analogue signals. Therefore not all combinations exist in regular operation. It is not possible to reduce the four comparators to three. On the one hand three comparators are able to generate 8 states but the distance between the edges must be equal. This can only be realized by 4 comparators. As a result, the course converter has a 3 bit resolution generated by 4 comparators. A digital decoder generates the 3 bit MSB.

The other two blocks of figure 3.17 are different from other approaches. Within the analogue switch array 8 analogue switches multiplex the four analogue inputs to two outputs - four switches for each output. The state of the analogue switches depends on the state of the coarse converter, or in other words on the detected eighth period. A digital decoder controls the analogue switch array in such a way that the analogue input signal is transformed into the output signals V_{f1} and V_{f2} . These output signals can be regarded as a

eightfold folded signal, which is mirrored each eighth period. The symmetry in this signal allows the multiple use of the following fine conversion.

The folding technique proposed in this work is distinguished from the published techniques in a number of ways:

- The coarse converter does not only generate some bits, it also controls the folding process.
- The analogue input signal waveform is maintained (within the eighth period).
- Two new waveforms are generated for symmetrical signal processing inside the ADC.
- This method does not use the slope of the comparators for the folding process.

Hence the proposed new method is not really comparable in spite of the same idea - the reduction of components and comparators by multiple use of the fine converter.

3.2.3 Nonlinear Signal Conversion

Most circuits today have the same signal processing structure. An amplifier exists at the interface to the sensor element and after amplification the signals are directly converted into the digital domain, where all signal processing is done by calculations. A DAC converts the calculated signals again into the analogue domain. Digital signal processing is a very powerful method, particularly if compensation of several non-ideals is required. But on the other hand the power consumption of such digital circuits can be quite high, especially if the clock frequency is high. For continuous time signal processing the clock frequency has to be high in order to satisfy the Nyquist criterion.

In special cases signal processing can be rather efficient, if a little more effort is spent on analogue signal processing. The advantages can be, for instance, a drastically reduced chip area of integrated circuits or, and this meets the purpose of this work, a considerable amount of energy can be saved. Hence, this concept employs the idea to substitute a lot of digital computation by analogue signal processing. As pointed out in this section no further power consumption is needed for the analogue signal processing.

Concerning the analogue sensor signals of sine and a second phase shifted sine two nonlinear input signals exist. For position measurement systems it is necessary to have linear output signals. That means the counts of length

or angle of the output signals always ideally have the same distance. The task for the measurement system is therefore to linearize the sensor element signals. As mentioned in the previous paragraph this task can be done within the analogue signal processing unit.

In general the position information can be provided by a single output signal of the sensor. One sine or cosine signal would be sufficient. There are some advantages if both signals are employed, particularly if direction information is only given if the correlation between the two signals is evaluated. This is valid for any position within one period. A second important benefit is the independence of the signal amplitude if the signal processing is based on the following equation 3.13.

$$V_{f1} = A_1 \cdot \sin \varphi \quad V_{f2} = A_2 \cdot \cos \varphi \quad (3.12)$$

$$\text{for } A_1 = A_2 \quad \Rightarrow \quad \frac{V_1}{V_2} = \frac{\sin \varphi}{\cos \varphi} = \tan \varphi$$

$$\Rightarrow \varphi = \arctan \frac{V_{f1}}{V_{f2}} \quad (3.13)$$

For ideal input signals V_{f1} and V_{f2} the output signal is an ideal, but nonlinear, arctan-function of the input signals. If this arctan-function is used over the complete period, the phase φ includes poles. Therefore, the arctan-function should only be used within a range of $\pm \frac{\pi}{4}$ to prevent exorbitant values. One possible way for signal processing may be:

- Parallel A/D conversion of both input signals
- Division in the digital domain (e.g. microprocessor)
- Arctan calculation (e.g. microprocessor) or processing by look-up-table with arctan values

This procedure has been used several times for position measurement systems. Digital computation is on the one hand suitable for low-voltage signal processing but on the other hand not a solution for low-power applications, especially if the signal processing can be done without any further power consumption inside the analogue signal processing. In order to anticipate the result, the division as well as the arctan calculation can be done within the ADC. The angle φ of equation 3.13 is linearized.

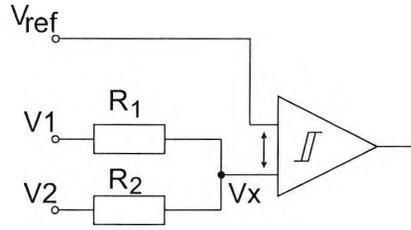


Figure 3.18: Simplified model for the resistor string

Consider the model of the A/D converter in figure 3.18, which is similar to figure 3.11. The included comparator represents one comparator, which can be each one at each node in the converter.

The basic function of the comparator leads to the condition in the switching point of $V_x = V_{ref}$. Rewriting equation 3.11 results in

$$\frac{R_2}{R_{tot}} = \frac{V_x - V_{f2}}{V_{f1} - V_{f2}} \quad (3.14)$$

with $R_{tot} = R_1 + R_2$. If the DC levels of V_{f1} and V_{f2} is assumed to be 0, then V_{ref} must also be chosen as 0, in order to adjust the A/D conversion between the zero crossing points of the sine formed input signals V_{f1} and V_{f2} . In fact the DC level is not zero, if an unipolar supply voltage is applied. Normally this is half of the power supply voltage V_{DD} . In this case V_{ref} or V_x must be chosen on the DC level of V_{f1} and V_{f2} . In any case the DC level and the reference voltage are subtracted by the comparator and in equation 3.14 V_x is ideally assumed to be 0. The ratio of the resistances can be expressed either in terms of R_1 or in terms of R_2 . The following equation 3.15 includes R_1 .

$$\frac{R_1}{R_{tot}} = \frac{1}{1 - \frac{V_{f2}}{V_{f1}}} = \frac{1}{1 + \frac{-\cos \varphi}{\sin \varphi}} = \frac{1}{1 + \cot \varphi} \quad for \quad V_x = V_{ref} \quad (3.15)$$

Linearization can be done if the resistor ratio of R_1/R_{tot} is also nonlinear. The calculation of the resistor network must be done for discrete values of φ , which depend on the required quantization. A general formulation of discrete values k of φ is given by the following expression 3.16.

$$\varphi_k = \frac{\pi/4}{n} \left(k - \frac{1}{2}\right) \quad for \quad k \in N^+ = \{1, 2, 3 \dots n\} \quad (3.16)$$

The highest resolution in equation 3.16 is represented by n . Due to the above discussed limitation of the arctan function, φ_k is mapped to $\pi/4$. Fur-

thermore this is the same range as the smallest symmetry of the folding signal (sec. 3.2.2.3). As a result the quantized φ_k refers to $\pi/4$ which fits to the coarse interpolation and an eighth of the input signal. The resolution Ψ of the overall system including folding and interpolation is given by

$$\Psi = \frac{P}{n_f \cdot n}, \quad (3.17)$$

where n_f of equation 3.17 is the resolution given by the folding unit and n specifies the resolution inside the smallest signal symmetry of the folded signal.

Based on equations 3.15 and 3.16 each resistor R_k of the A/D converter can be calculated. Each resistor has a different value. The resistors are calculated by the following expression 3.18.

$$R_k = R_{tot} \cdot \frac{1}{1 + \frac{\cos \varphi_k}{\sin \varphi_k}} - R_{tot} \cdot \frac{1}{1 + \frac{\cos \varphi_{k-1}}{\sin \varphi_{k-1}}} \quad (3.18)$$

Equation 3.18 subtracts always the previous resistor value based on φ_{k-1} . This is not valid for the first resistor and casually $\varphi = 0$ would cause an infinite result. Therefore the calculation of R_k becomes case dependent as given by

$$R_k = \begin{cases} R_{tot} \cdot \frac{1}{1 + \cot \varphi_k} & \text{if } k = 1 \\ R_{tot} \cdot \left\{ \frac{1}{1 + \cot \varphi_k} - \frac{1}{1 + \cot \varphi_{k-1}} \right\} & \text{if } k \geq 2 \end{cases} \quad (3.19)$$

All resistors values result from equation 3.19 without the last one of the chain. This resistor R_{k+1} can be calculated by

$$R_{k+1} = R_{tot} - \sum_{k=1}^n R_k \quad (3.20)$$

The value of the last resistor of the chain is in the range of the sum of all other resistors. This can be also understood as a level shift up to $V_{DD}/2$.

Within this section linearization was introduced. It refers to a reproduction of the input signal. As long as the conditions of the input signal do not change, the linearization is ideal. In principle this method can be applied for any waveform. If for instance the input waveform would be a triangle, the resistor values would be linearly weighted. If the input signal has a fixed distortion, linearization can be obtained by taking harmonics into account.

3.3 Reference Voltage Generation

In the preceding sections 3.1.3 and 3.2.3 a reference voltage has been applied to the instrumentation amplifier and to the A/D converter. This reference voltage depends on the input signal or the sensor element output signals, respectively.

The DC level of the sensor element output is very often $V_{DD}/2$. For the magneto resistive sensor element (sec. 3.1.1) the reference voltage is given by equation 3.1 assuming that the sensor element is voltage driven. In current mode the DC level could be different.

Due to the instrumentation amplifier the signal processing becomes independent of the operating point of the sensor element, because the output level of the amplifier only depends on the reference voltage adjustment, if the sensor and the amplifier offset is neglected. As a result, a precise reference voltage generation in the circuit is required, which effects only on the analogue circuit. All units of the circuit are related to one reference.

Two possibilities for voltage generation exist in principle. First, a fixed temperature and power supply independent reference voltage can be used, as it can be generated by a bandgap reference voltage generator, for instance. Second, a floating, power supply dependent and temperature independent reference voltage can be used. The problem of the first solution is that advantages of larger dynamic ranges could not be used. The latter solution is preferred, because the reference voltage can follow the power supply voltage. Then larger amplitudes can be processed in the circuit. The voltage generation is depicted in figure 3.19.

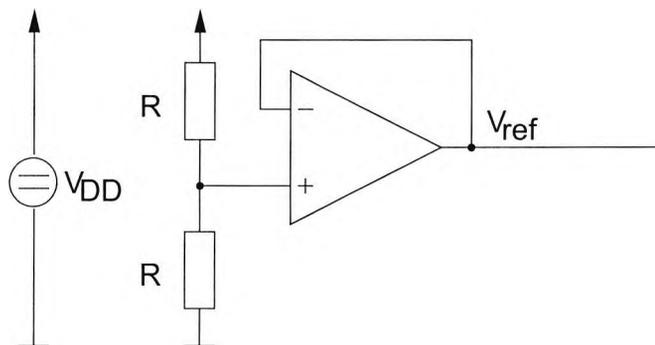


Figure 3.19: Reference voltage generation

This reference voltage V_{ref} is temperature independent if it is assumed that no temperature gradient between the resistors exists. By layout tech-

niques the offset and the temperature dependent offset can be minimised. Large resistor areas are required on the chip.

3.4 Output Interface

Various types of interfaces are used in position measurement systems. All of them include the position information. But not all position measurement systems provide in addition a direction information. Traditional output interfaces are [4]:

- analogue potentiometer output
- absolute value
- incremental value
- protocol based outputs (e.g. bidirectional)

For this work the incremental output interface was chosen in order to provide a suitable interface for evaluating the system with reasonable effort. Typical for this interface is that the output produces two signals with a phase shift of 90 degrees, in response to the analogue input. This phase shift can be either $+90^\circ$ or -90° . In other words the incremental output is the digital counterpart of the analogue input signal. An incremental output interface is shown in figure 3.20.

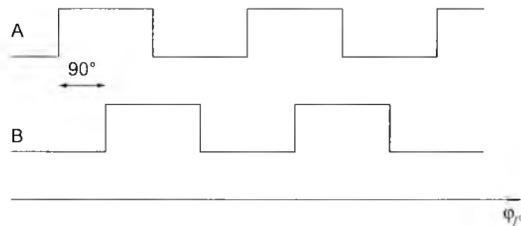


Figure 3.20: Incremental output signal

For position measurement systems with non enhanced resolution the output signal as shown in figure 3.20 can easily be generated by two analogue comparators which sense the sine waveforms of figure 3.2. Then the frequency of the analogue and the digital signals are equal.

For systems with enhanced resolution, as described in section 3.2, a digital encoder is necessary. This encoder can be placed at the output of the ADC (chapter 3.2.2). At the output of the ADC the signal is decoded into a so-called thermometer code, as it is typical for this kind of flash converters.

Chapter 4

Modeling

4.1 Magneto Resistive Sensor Model

A change of the conductance as a function of an extrinsic magnetic field is the phenomenon of the magneto resistive effect. The anisotropic magneto resistive (AMR) effect appears in ferro magnetic materials like Permalloy which evince a magnetization on their own. In figure 4.1 a magneto resistive resistor is depicted.

M is the direction of the magnetization and i is the current through the resistor. The magnetic fields H_y and H_x turn the direction of the magnetization M by the angle Θ .

The first developed model for the anisotropic magnetoresistive effect was expressed by the Voigt-Thomson equation [58],[59]. This model describes the correlation between the direction of the magnetization and the direction of the current for a very simple stripe of Permalloy. Most of today's AMR sensor elements have aluminium strips on top of the thin film of Permalloy. This is shown in figure 4.2

These aluminium strips turn the direction of the current by 45° with respect to the direction of the magnetization due to the fact that the conductivity of aluminium is essentially higher than Permalloy. The reason of

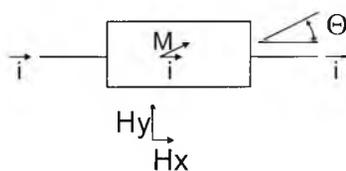


Figure 4.1: Magneto resistive resistor

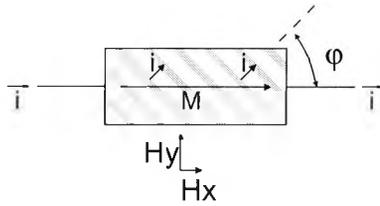


Figure 4.2: Magnetoresistor with barberpol structure

this direction change is the shift of the operating point of the sensor element. For magneto resistive sensor elements with a barberpol structure the resistance is given by

$$R(\varphi) = R_0 - \frac{\Delta R}{2} \cdot (1 \pm \sin(2\varphi)) \quad (4.1)$$

where R is the resistance, R_0 is the magnetoresistance without a magnetic field, ΔR is the maximum change of the resistance and φ is the angle between the direction of the magnetisation and the current. R_0 depends on the technology of the magnetoresistive film, if no magnetic field is applied.

Of interest in terms of power consumption is R_0 and ΔR . Typical ranges of R_0 are between some $k\Omega$ and hundreds of $k\Omega$. For low-power systems high ohm sensors are used. Concerning ΔR , a change of about 2% is typical and has therefore a negligible influence.

In equation 4.1 φ depends on the extrinsic magnetic fields. Following the implicit equation in terms of φ expresses the correlation between the magnetic fields and φ .

$$0 = H_x \cdot \tan(\varphi) + H_0 \cdot \sin(\varphi) - H_y \quad (4.2)$$

where H_0 is the characteristic field which depends on the technology and H_y as well as H_x , the extrinsic magnetic fields, which take effect on the sensor element as shown in figure 4.2. In order to solve equation 4.2 iterative methods like Newton-Raphson are used. Convergence problems exist for special relations of the applied magnetic fields. As proposed by [60] a method of bypassing can be implemented for the mixed-domain simulation of sensor element and electronic circuit.

The dependence of the temperature of R_0 is given by

$$R_0 = R_{25^\circ} \cdot (1 + \alpha_{R0} \cdot (T - 25^\circ C)) \quad (4.3)$$

where R_{25° is the resistance at room temperature and α_{R0} is the first order temperature coefficient. The second order temperature coefficient is

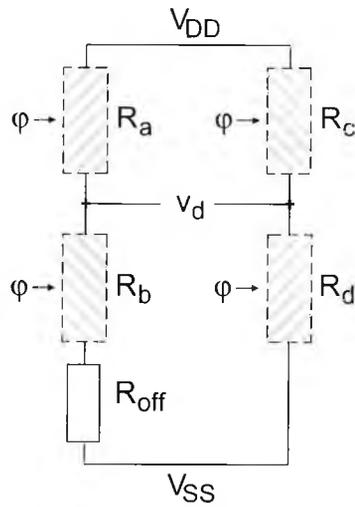


Figure 4.3: Wheatstone bridge with offset

negligible. Beside R_0 , ΔR is also temperature dependent. In other words this is the effect that the amplitude of the sensor element decreases with increasing temperature. The following equation 4.4 expresses the correlation considering the first order temperature coefficient.

$$\Delta R = R_0 \cdot r_{hub} \cdot (1 + \alpha_{\Delta R} \cdot (T - 25^\circ C)) \quad (4.4)$$

where r_{hub} is the hub of the resistance and $\alpha_{\Delta R}$ is the temperature coefficient.

So far a single magnetoresistor strip was considered. The sensors for position measurement systems normally provide a differential output signal in order to suppress common mode disturbances. Therefore four sensor elements are arranged as a Wheatstone bridge as shown in figure 4.3.

The Wheatstone bridge consists of four magnetoresistors and in addition a resistor for the offset is modeled. For calculations this resistor can be either positive or negative. The direction of the barberpol stripes of the magnetoresistors R_a and R_d as well as R_b and R_c are equal in respect of the extrinsic magnetic field vector, here represented as the resulting angle φ . If the voltage on the left hand half bridge increases, the voltage on the right hand half bridge decreases by the same magnitude. This doubles the effect at the differential output. Regarding equation 4.1 the magnetoresistors R_a and R_d have the same sign as R_b and R_c , respectively.

The model for the offset V_{off} contains two parts, representing the power supply and temperature dependence. This is given by

$$V_{off} = (V_{DD} - V_{SS}) \cdot (d_{off} + \alpha_{off}(T_s - 25^\circ C)) \quad (4.5)$$

where d_{off} is the power supply dependent offset, α_{off} is the power supply dependent temperature coefficient of the offset and T_s is the temperature in $^\circ C$ of the sensor. Using the offset voltage of equation 4.5, the offset resistance r_{off} can be calculated by the following relationship 4.6.

$$r_{off} = \frac{V_{off}}{V_{DD} - V_{SS} - V_{off}} \cdot (R_a + R_b) \quad (4.6)$$

Between the two branches of the Wheatstone bridge the differential output signal V_d can be calculated by

$$V_d = V_{SS} + V_{off} + (V_{DD} - V_{off} - V_{SS}) \frac{R_b}{R_a + R_b} - (V_{DD} - V_{SS}) \frac{R_c}{R_c + R_d} \quad (4.7)$$

This model can be used for large signal as well as for transient analysis of this sensor element and for investigations of the system. There is no explicit small signal model for very high frequencies given, because the bandwidth is many orders of magnitude higher than the bandwidth of the electronic circuit.

Considering the sensor as a source of error, the following items must be taken into account:

- Offset
- Amplitude differences between sine and cosine
- Phase error between sine and cosine
- Distortion

These influences can be simulated. Furthermore, these are items implemented in the error model for the system architecture.

4.2 Error Model for the System Architecture

4.2.1 Mismatch Error of the Resistor String

In section 3 the system architecture was introduced. At the interface between the analogue and the digital domain, the overall error of the analogue part can be considered. A number of errors are fed through the system - for example

the overall offset. Therefore worst case inspections for non-correlated errors are done at the point where all errors are summed.

Figure 3.10 of the proposed flash converter is considered again. At each comparator the error sum at the analogue signal is compared with the reference voltage V_{ref} . Due to the fact that the comparators switch if $V_{x_n} = V_{ref}$, the overall error is represented by the phase error. In other words, each error contributes to a shift of the voltage V_{x_n} from the ideal value. This shift has a phase counterpart.

One important issue is related to the resistor ladder network. As is typical of all similar types of A/D converter, the matching of the resistors determines the resolution limit of such converters. In the case of the proposed A/D converter the resistor network is nonlinear. Section 3.2.3 describes the method of linearization of the input signal by weighting the resistors non-linearly. The method is based on an arctan-function, derived from the two input signals V_1 and V_2 . For repetition

$$V_1 = A_1 \cdot \sin \varphi \quad V_2 = A_2 \cdot \cos \varphi \quad (4.8)$$

are taken as the ideal signals. Then the ideal phase φ can be written as

$$\varphi = \arctan \frac{V_1}{V_2} \quad (4.9)$$

In order to derive an equation of the error caused by the resistor matching, equation 4.9 must be expressed in terms of R_1 and R_2 . The condition for the switching point is $V_x = V_{ref}$. This voltage is strongly correlated to DC voltage of V_1 and V_2 . For simplicity V_{ref} can be seen as zero. Based on the current through the resistors it can be written

$$\left| \frac{V_1}{V_2} \right| = \left| \frac{R_1}{R_2} \right| \quad (4.10)$$

Substituting V_1 and V_2 in equation 4.9 by equation 4.10 gives

$$\varphi = \arctan \frac{R_1}{R_2} \quad (4.11)$$

Errors of the resistors are not correlated. Therefore the absolute phase error for each phase can be derived by

$$\begin{aligned} \Delta\varphi_{max} &= \left| \frac{\partial\varphi}{\partial R_1} \Delta R_1 \right| + \left| \frac{\partial\varphi}{\partial R_2} \Delta R_2 \right| \\ &= \left| \frac{R_2}{R_1^2 + R_2^2} \cdot \Delta R_1 \right| + \left| \frac{R_1}{R_1^2 + R_2^2} \cdot \Delta R_2 \right| \end{aligned} \quad (4.12)$$

As a result, the error is independent of the total resistance $R_{tot} = R_1 + R_2$, which is not obvious from the equation itself. But if for instance the unit of R_1 and R_2 is $k\Omega$ or $M\Omega$ the units are cut. The unit of ΔR_1 and ΔR_2 can be taken in the same range. For example the error may be 2% of the resistor value. Hence, the error caused by the resistor ladder can only be reduced if ΔR_1 and ΔR_2 is kept small. This can only be achieved at a layout level, if the resistor die area is large, because the resistor value for integrated resistors is given by $R = L/W \cdot R_{square}$, where L is the resistor length, W is the resistor width and R_{square} is the normalised resistance per square.

4.2.2 Iterative Overall Error Model

4.2.2.1 Basic Functionality

In the previous section 4.2.1 the error caused by the resistor string was discussed in detail and an explicit expression was found for the error. If further errors are considered in the equation an explicit solution with respect to the angle φ is no longer possible. That means the resulting equation is implicit. Such equations are solved by iterative approaches like the Newton algorithm. Various errors influence the accuracy of the system. All considerations are based on the origin that $V_x = V_{ref}$ and that the overall error is totally represented by a corresponding phase error. Figure 4.4 depicts the error sources.

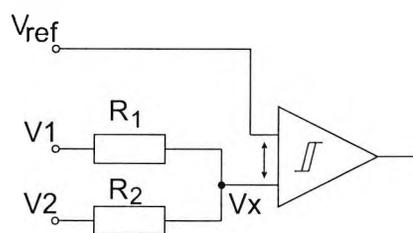


Figure 4.4: Model of error sources for the flash converter

In detail the errors are as follows:

- Mismatch of the resistor string
- Offset of the reference voltage V_{ref}
- Offset and Hysteresis of the comparators
- Offset of the input signals V_{f1} and V_{f2}
- Difference of the amplitudes V_{f1} and V_{f2}

- Phase error between V_{f1} and V_{f2}
- Distortion of the input signals

The voltage reference generation was introduced in section 3.3. V_{ref} is applied to the input amplifiers, the comparators in the folding unit and the comparators of flash converter. The resistor matching as well as the offset of the voltage follower contribute to the error $\pm\Delta V_{ref}$ of the reference voltage. In addition to ΔV_{ref} the comparators of the flash converter have an offset $\pm V_{off,comp}$ and a fixed hysteresis V_{hys} . All errors from the input signals V_{f1} and V_{f2} are a combination of sensor element errors and the preceding signal processing components. If these errors are accumulated at the nodes V_{f1} and V_{f2} all static errors are taken into account. In detail the input signals show offsets $V_{off,v1}$ and $V_{off,v2}$, a phase error $\pm\epsilon$ and deviations of the amplitude $\pm\Delta A_{v1}$ and $\pm\Delta A_{v2}$. Signal distortion can be taken into account if $V_{f1} \neq \sin$ and $V_{f2} \neq -\cos$ as is assumed for the calculation of the resistor string. In order to derive an equation for the overall error, equation 3.14 is solved for $V_x = 0$, resulting in

$$0 = \frac{R_1}{R_{tot}}V_{f2} + \left(1 - \frac{R_1}{R_{tot}}\right)V_{f1} \quad (4.13)$$

Adding all mentioned errors to equation 4.13 and substituting sine and cosine for V_{f1} and V_{f2} , respectively, leads to the following model equation 4.14 for the overall error calculation.

$$\begin{aligned} 0 &= \left(\frac{R_1}{R_{tot}} + \frac{\Delta R_1}{R_{tot}}\right) \cdot (-A_c)(1 + \Delta A_c) \cdot \cos(\varphi) + V_{off,c} \dots \\ &+ \left(1 - \frac{R_1}{R_{tot}} + \frac{\Delta R_1}{R_{tot}}\right) \cdot A_s(1 + \Delta A_s) \cdot \sin(\varphi + \epsilon) - V_{off,s} \dots \\ &- \Delta V_{ref} + V_{off,comp} + V_{hys} \end{aligned} \quad (4.14)$$

For the determination of the maximum error all errors must be added for the worst case to the error model of equation 4.14. The worst case is not obvious from the given error parameters. For the resistors the errors ΔR_1 and ΔR_2 must be contrary. This is the same for the amplitude errors ΔA_{v1} and ΔA_{v2} as well as for the offsets $V_{off,v1}$ and $V_{off,v2}$. At the inputs of the comparator $V_{off,c}$ and V_{hys} must have the same sign but should also be opposite to the sign of ΔV_{ref} .

4.2.2.2 Folding Procedure

Ideal Signal processing

The model of section 4.2.2.1 does not mirror the behavior of the system but explains the basic functionality and the interaction of the special topology of the A/D converter and the input signals. In the last instance, this model is only valid for a range of values. With respect to the phase of the input signal validity is only given for $2\phi/N_f$, where the number of folding N_f is 8 as long as the signal transformation of the folding circuit is not considered.

In section 3.2.2.3 the signal folding concept was introduced. For modeling the architecture as shown in figure 3.13 the model is separated into the same parts. Doing this enables a good verification with an electrical simulation.

At first, it should be stated that the analogue input signals drive the folding unit. It is necessary to declare these signals as

$$v_{spi} = -v_{sni} = \sin\left(\frac{2\pi}{N}N_x\right) \quad (4.15)$$

$$v_{cpi} = -v_{cni} = \cos\left(\frac{2\pi}{N}N_x\right) \quad (4.16)$$

where N is the period which can be the position, an angle, the time or any other unit. N_x is the counting variable.

The coarse converter consists of four analogue comparators. Their switching characteristic can be described by

$$k_{p1i} = \begin{cases} 0 & \text{if } v_{spi} > 0 \\ 1 & \text{otherwise} \end{cases} \quad (4.17)$$

$$k_{p2i} = \begin{cases} 0 & \text{if } v_{spi} > v_{cpi} \\ 1 & \text{otherwise} \end{cases} \quad (4.18)$$

$$k_{p3i} = \begin{cases} 0 & \text{if } v_{cpi} > 0 \\ 1 & \text{otherwise} \end{cases} \quad (4.19)$$

$$k_{p4i} = \begin{cases} 0 & \text{if } v_{cpi} > v_{sni} \\ 1 & \text{otherwise} \end{cases} \quad (4.20)$$

All of the four comparators have only two states which drive the digital segment decoder. For a folding value of $N_f=8$ this decoder must have eight states. The behaviour of the decoder, which is controlled by k_{p1i} to k_{p4i} , is as follows:

$$swi = \begin{cases} 1 & \text{if } k_{p1i} = 0 \wedge k_{p2i} = 1 \wedge k_{p3i} = 0 \wedge k_{p4i} = 0 \\ 2 & \text{if } k_{p1i} = 0 \wedge k_{p2i} = 0 \wedge k_{p3i} = 0 \wedge k_{p4i} = 0 \\ 3 & \text{if } k_{p1i} = 0 \wedge k_{p2i} = 0 \wedge k_{p3i} = 1 \wedge k_{p4i} = 0 \\ 4 & \text{if } k_{p1i} = 0 \wedge k_{p2i} = 0 \wedge k_{p3i} = 1 \wedge k_{p4i} = 1 \\ 5 & \text{if } k_{p1i} = 1 \wedge k_{p2i} = 0 \wedge k_{p3i} = 1 \wedge k_{p4i} = 1 \\ 6 & \text{if } k_{p1i} = 1 \wedge k_{p2i} = 1 \wedge k_{p3i} = 1 \wedge k_{p4i} = 1 \\ 7 & \text{if } k_{p1i} = 1 \wedge k_{p2i} = 1 \wedge k_{p3i} = 0 \wedge k_{p4i} = 1 \\ 8 & \text{if } k_{p1i} = 1 \wedge k_{p2i} = 1 \wedge k_{p3i} = 0 \wedge k_{p4i} = 0 \end{cases} \quad (4.21)$$

This model of equation 4.21 can be taken for the signal transformation of the input signal. At the output of the transformation the two new signals V_{f1} and V_{f2} are built.

For the calculation of the resistor network, which is also designed for $2\pi/8$ signal processing, the phase can be shaped for the resistance calculation. This procedure can be applied to the equations 3.16 and 3.15. According the calculation of the nonlinear resistance arrangement, the phase is shaped in N_f parts by a sawtooth waveform. The generation is given by

$$\phi = \begin{cases} N_x & \text{if } swi = 1 \\ \frac{N}{4} - N_x & \text{if } swi = 2 \\ N_x - \frac{N}{4} & \text{if } swi = 3 \\ \frac{N}{2} - N_x & \text{if } swi = 4 \\ N_x - \frac{N}{2} & \text{if } swi = 5 \\ \frac{3N}{4} - N_x & \text{if } swi = 6 \\ N_x - \frac{3N}{4} & \text{if } swi = 7 \\ N - N_x & \text{if } swi = 8 \end{cases} \quad (4.22)$$

If the shaped phase is used the following equation 4.23 results.

$$R_1(\phi) = R_{tot} \cdot \frac{1}{1 + \cot(\frac{2\pi}{N}\phi)} \quad (4.23)$$

This equation linearizes the following expression which is valid for ideal input signals.

$$0 = \left(1 - \frac{R_1}{R_{tot}}\right) \cdot \sin(\alpha_i) + \frac{R_1}{R_{tot}} \cdot \cos(\alpha_i) \quad (4.24)$$

where R_1 is given by figure 3.18, R_{tot} is the total resistance between the voltages V_{f1} and V_{f2} and α_i is the input referred angle of the sensor signal, which must be solved. This equation can be taken for solving errors, where it is of interest to calculate the deviations of the non-ideal signal. If for instance the interpolation value is $n_f \cdot n = 64$ over one complete input period, the ideal and linearized signal waveform is as shown in figure 4.5.

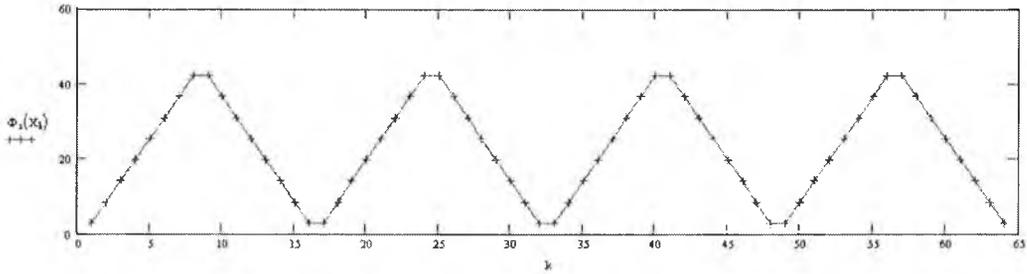


Figure 4.5: Ideal input referred angle

On the x-axis the variable k counts 64 steps. Each step corresponds to one increment at the output on the AB-signal (sec. 3.4). The resolution here is 64 and corresponds to a 16 times higher frequency at the output compared with the analogue input signal. The angle on the y-axis rises up and falls down linearly. The increment is $45^\circ/n=45^\circ/8$. Any resolution is here ideally possible. But in the case of taking errors into account the resolution is limited. This can be investigated by using the described models in the case of ideal signals and by inserting all errors as discussed at the beginning of this section 4.2.2.1.

Non-Ideal Signal processing

Non ideal input signals which are not distorted are included in the model equation 4.14. While folding the input signal, the analogue switches always select one of the non-ideal input signals depending on the state of the coarse converter. Offset, differences between the amplitudes and phase errors can cause steps on the signals V_{f1} and V_{f2} . The reason is that these non-ideal influences are different between the sine and cosine signals. As a result, these influences depend on the switching state of the coarse converter. If the amplitude is defined as $s_A = A_s \cdot (1 + \Delta A_s)$ and c_A for the cosine then the amplitudes of the voltage V_{f1} and V_{f2} are given by

$$A_1 = \begin{cases} s_A & \text{if } sw = 1 \vee sw = 4 \vee sw = 5 \vee sw = 8 \\ c_A & \text{if } sw = 2 \vee sw = 3 \vee sw = 6 \vee sw = 7 \end{cases} \quad (4.25)$$

$$A_2 = \begin{cases} s_A & \text{if } sw = 2 \vee sw = 3 \vee sw = 6 \vee sw = 7 \\ c_A & \text{if } sw = 1 \vee sw = 4 \vee sw = 5 \vee sw = 8 \end{cases} \quad (4.26)$$

Comparable to the calculation of the amplitude, the offset voltage is switched in dependence of the state of the coarse converter. The offsets V_{o1} and V_{o2} of the voltages V_{f1} and V_{f2} can be expressed as follows:

$$V_{o1} = \begin{cases} V_{offs} & \text{if } sw = 1 \vee sw = 4 \vee sw = 5 \vee sw = 8 \\ V_{offc} & \text{if } sw = 2 \vee sw = 3 \vee sw = 6 \vee sw = 7 \end{cases} \quad (4.27)$$

$$V_{o2} = \begin{cases} V_{offs} & \text{if } sw = 2 \vee sw = 3 \vee sw = 6 \vee sw = 7 \\ V_{offc} & \text{if } sw = 1 \vee sw = 4 \vee sw = 5 \vee sw = 8 \end{cases} \quad (4.28)$$

where V_{offs} and V_{offc} are the offset voltages of the sine and the cosine, respectively.

If equation 4.14 is used, the sine and cosine waveforms are fixed. Another way would be to define these waveforms as V_{f1} and V_{f2} . Any waveform could be defined for these voltages. This can be done if signal distortion is considered. But if equation 4.14 is taken, an additional phase variable can be modeled in order to switch between sine and cosine and their inverted counterparts. These phase variables α_1 and α_2 are also a function of the state of the coarse converter. They can be calculated by relation 4.29

$$\alpha_1 = \begin{cases} 0 & \text{if } swi = 1 \\ \frac{\pi}{2} & \text{if } swi = 2 \\ -\frac{\pi}{2} & \text{if } swi = 3 \\ 0 & \text{if } swi = 4 \\ \pi & \text{if } swi = 5 \\ -\frac{\pi}{2} & \text{if } swi = 6 \\ \frac{\pi}{2} & \text{if } swi = 7 \\ \pi & \text{if } swi = 8 \end{cases} \quad \alpha_2 = \begin{cases} -\frac{\pi}{2} & \text{if } swi = 1 \\ \pi & \text{if } swi = 2 \\ \pi & \text{if } swi = 3 \\ \frac{\pi}{2} & \text{if } swi = 4 \\ \frac{\pi}{2} & \text{if } swi = 5 \\ 0 & \text{if } swi = 6 \\ 0 & \text{if } swi = 7 \\ -\frac{\pi}{2} & \text{if } swi = 8 \end{cases} \quad (4.29)$$

Equation 4.14 which does not cover the folding behaviour it can be enhanced by all parameters which are switched. The switched parameters are a function of the variable N_x . This results in

$$\begin{aligned} 0 &= \left(\frac{R_1(N_x)}{R_{tot}} + \frac{\Delta R_1}{R_{tot}} \right) \cdot A_2(N_x) \cdot \cos(\alpha_e + \alpha_2(N_x)) + V_{o2}(N_x) \dots \\ &+ \left(1 - \frac{R_1(N_x)}{R_{tot}} + \frac{\Delta R_1}{R_{tot}} \right) \cdot A_1(N_x) \cdot \sin(\alpha_e + \alpha_1(N_x) + \epsilon) - V_{o1}(N_x) \dots \\ &- \Delta V_{ref} + V_{off,comp} + V_{hys} \end{aligned} \quad (4.30)$$

where α_e represents the input referred phase error. Equation 4.30 is regarding α_e implicit and has therefore to be solved by an iterative algorithm. As an example the following values are assumed: $A_s = A_c = 0.6$ V, $R_{tot} = 1$ M Ω , $\Delta A_s = -\Delta A_c = 5\%$, $V_{offs} = -V_{offc} = 0.06$ V, $V_{offref} = V_{offcomp} = V_{hys} = 5$ mV, $\epsilon = 2\pi * 2\%$ and $\Delta R_1 = 10$ k Ω . Solving equation 4.30 with $N_x = 512$ and a resolution of $\Psi = 64$ results in an input referred phase that is depicted in figure 4.6.

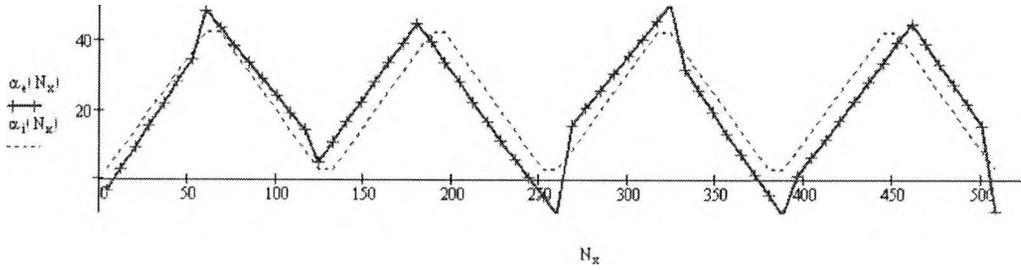


Figure 4.6: Input referred phase for non-ideal paramters

For comparison, figure 4.6 also contains the run of the ideal curve α_i . It depends on the offset if the curve is above or below the ideal curve progression. Due to the different offsets of sine and cosine, discontinuities exist at each $\frac{\pi}{4}$ or here within the simulation at each $\frac{512}{8}$ increment.

Such a result as shown in figure 4.6 does not take into account that the error of the resistance ΔR_1 has stochastic values. It can either be positive or negative and in addition its value is non-constant. The model for ΔR_1 can also be based on matching considerations. Depending on the technology and layout R_1 would vary by a fixed factor. ΔR_1 can be modeled as

$$\Delta R_1(N_x) = (-1)^{N_x} \cdot R_1(N_x) \cdot f_{\Delta R_1} \quad (4.31)$$

where $f_{\Delta R_1}$ is the factor of ΔR_1 in percent. For worst case calculations ΔR_1 alters with its sign. If this need not be considered the absolute value can be taken instead.

An alternation of the sign is also given for the offset, if the worst case is assumed. The resulting model is similar to the change of the resistance error. It is given by

$$V'_{offcomp} = (-1)^{N_x} \cdot V_{offcomp} \quad (4.32)$$

Calculations which incorporate the alternation of the sign entail a chatter of values inside each $\frac{\pi}{4}$ increment.

Concerning the hysteresis, the folding process does not have any effect on the sign of the hysteresis as long as the input signals continue in one direction of movement. A change of the movement direction is not implemented. It would lead to a further inaccuracy.

Within this model the inherent offset of the comparator of the coarse converter is disregarded. The discontinuous magnitude of the curve is influenced

by the offset. Nevertheless it can be disregarded because the thresholds for AD conversion are not effected.

4.2.3 Differential Error and Integral Nonlinearity

A flash A/D converter as proposed in section 3.2.2 is defined by a few parameters. They can be separated into two categories. Here only the static errors and not the dynamic ones are considered, because errors such as aperture jitter are related to sampling converters.

The model formulations of the preceding section 4.2.2 refer to both input signal errors and errors of the converter. With these parameters it is possible to investigate separately or simultaneously the output errors. Furthermore the output errors can also be related to corresponding input values.

In order to evaluate the accuracy with respect to the resolution and the power supply voltage simultaneous analyses is necessary. If errors of the input signals are not taken into account, the folding A/D converter could be characterized. The errors can be evaluated by the differential nonlinearity (DNL) and the integral nonlinearity (INL).

The DNL error is the deviation of the smallest step size. The smallest step sizes is one LSB. Any error causes an increase or a decrease of the increment. For the folding A/D converter the DNL error is defined within each folding segment. If for this sensor system the errors are expressed in terms of a corresponding input error of α_e the *DNL* is given by

$$DNL_k = \alpha_{e_k} - \alpha_{e_{k-1}} \quad (4.33)$$

where k is the counting variable which can be in any domain like time, phase or position. Taking the same example of the previous section with the result of figure 4.6, the DNL error can be calculated by equation 4.33. The result is depicted in figure 4.7.

In figure 4.7 the DNL error was normalised to 1 LSB. Nearly all values have a deviation around +1 or -1, respectively. If the DNL exceeds one LSB the converter is no longer monotonic. The values that are larger than one LSB are not values which are inside one folding segment. Assuming an ideal converter the neighbouring points between two abutting segments have a DNL error of zero because they have equal values. Hence the definition range of the folding converter must be taken into account and the higher values between two segments can be disregarded.

Very useful for determination of the accuracy is the integral nonlinearity error, because the INL error is defined as the deviation of the ideal value as given by

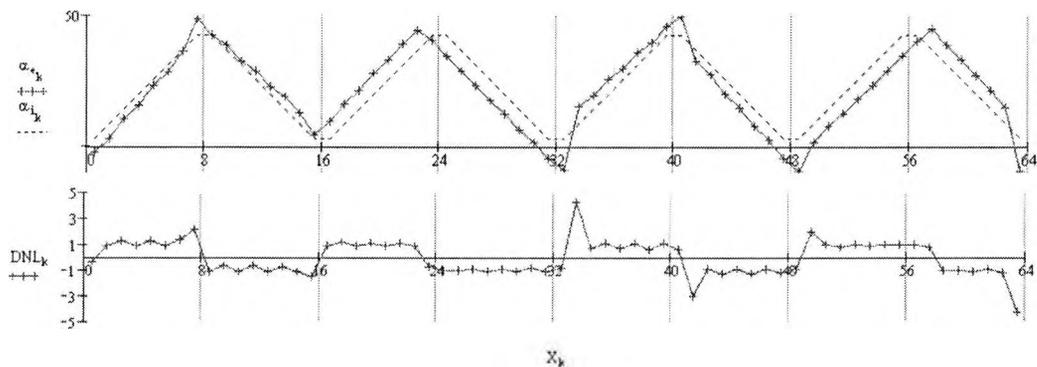


Figure 4.7: Differential nonlinearity

$$INL_k = \alpha_{e_k} - \alpha_{i_k} \quad (4.34)$$

where α_{i_k} is the ideal input referred angle and k is the counting variable. The following figure 4.8 shows the result of the example of the previous section normalised to one LSB.

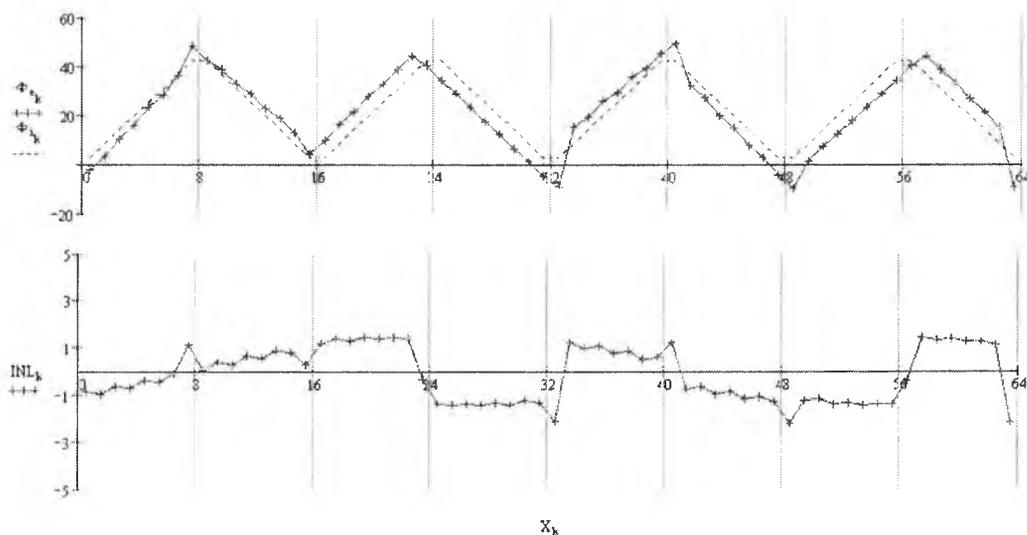


Figure 4.8: Integral nonlinearity

Comparable with the DNL analysis the INL error curve includes steps caused by the discontinuity signal processing of the folding unit. The INL error is an error with the same period as the related input signal. Its magnitude depends on the ratio of the signal amplitude to the offset. As a rule

of thumb 10% corresponds to 1 LSB. Coming back to the example, the amplitude is 0.6 V and the offset 0.06 V and neglecting all other effects, results in figure 4.8 and is between ± 1 . This is expected for a normalised curve. If the folding segments are put continuously together, a curve similar to a sine wave can be generated. The same result can be generated by applying the absolute value to equation 4.34. Then two half sine waves would be the result.

Normally, for the DNL and INL error, the offset and the gain error are subtracted before determining the values for an A/D converter. Within this work all errors are considered and the quality of the system are expressed in terms of DNL and INL.

Referring to low-voltage aspects, the DNL and the INL errors are higher because of the smaller amplitudes. Ideally the interpolation operates independently of the amplitude. If all errors are assumed zero the amplitude or the difference between V_{f1} and V_{f2} , respectively, can be very small.

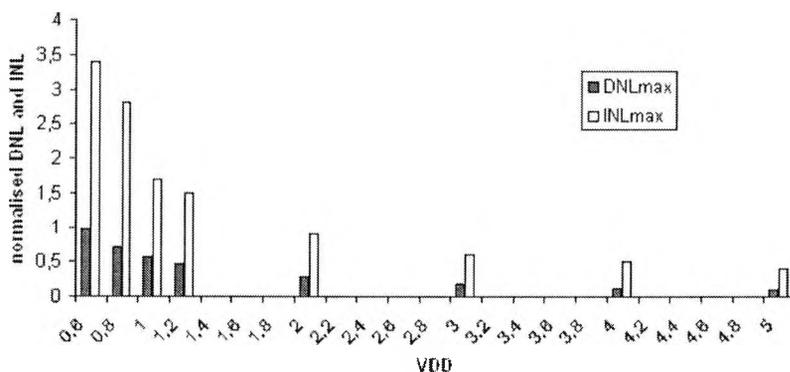


Figure 4.9: Influence of power supply voltage on DNL and INL

The ratio of the voltage drop across the resistor ladder of the A/D converter to the error voltages of the converter and the input signals determines the achievable accuracy of the system. If the power supply voltage is minimised, the voltage across the resistor ladder is limited. Figure 4.9 includes the result of an investigation of this ratio, where the errors are taken from the example of the previous section and are fixed.

Figure 4.9 shows an asymptotic curve run against zero for increasing amplitudes and a significant, nonlinear increase of the curve can be seen for small ratios.

4.2.4 Position Error

As previously introduced in section 4.2.2, the model of the system architecture enables investigations of the system by an input error referred consideration. This is a useful method as long as equation 4.30 is fulfilled. That means that the implicit expression on the right hand side must be zero. An iterative algorithm is needed in order to calculate angles for which this expression is zero.

In reality the input signals V_{f1} and V_{f2} have fixed phase relations. Another method for evaluation is to calculate the overall error voltage for a given phase. This can be formulated as follows:

$$\begin{aligned}
 P_t(P_x) = & \left(\left(\frac{R_1(P_x)}{R_{tot}} + \frac{\Delta R_1}{R_{tot}} \right) \cdot A_2(P_x) \cdot \cos(\alpha_e + \alpha_2(P_x)) + V_{o2}(P_x) \dots \right. \\
 & + \left(1 - \frac{R_1(P_x)}{R_{tot}} + \frac{\Delta R_1}{R_{tot}} \right) \cdot A_1(P_x) \cdot \sin(\alpha_e + \alpha_1(P_x) + \epsilon) - V_{o1}(P_x) \dots \\
 & \left. - \Delta V_{ref} + V_{off,comp} + V_{hys} + P_x \right) \quad (4.35)
 \end{aligned}$$

where P_t is the position corresponding voltage at each tap of the converter, P_x is the index variable which is equal to the sum of the ideal voltage increments at position x . All other parameters are illustrated in section 4.2.2.1. Without P_x on the right hand side, equation 4.35 would calculate the error voltage around zero. If P_x is added, this function delivers a position corresponding voltage. An extension of this equation can be a multiplication by $360^\circ/N$, where N is the total number of increments. Then the output gives the position corresponding to the angle. In the following figure 4.10 the output is referred to a position over a period of 1 mm for the example

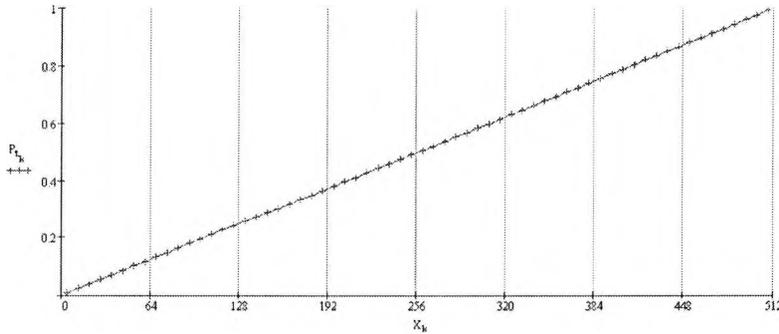


Figure 4.10: Steady increase of the position

of the previous section. The errors in this curve are not obvious. DNL and INL analyses can also be applied to this curve.

If distortion should be considered, the models of equations 4.30 and 4.35 can be extended. Instead of only operating with the fundamental wave of sine and cosine, harmonics can be added. The amplitudes of the harmonics caused by the electronics can be estimated by the analysis of the distortion of the output of the instrumentation amplifier (see figure 2.38). Furthermore the sensor front-end consisting of the sensor element and the magnetic gauge may contribute to the overall signal distortion. This depends on the sensor element itself and adjustment mismatches with respect to the gauge. Also disturbing magnetic fields could be a major issue.

Noise has not been considered within this model. This is not necessary. The total noise at each tap of the resistor ladder must be smaller than the hysteresis of the comparator. This is an important requirement for proper functionality. Hence no noise model need to be used.

Chapter 5

System Evaluation

5.1 Experimental Results of Signal Conditioning Unit

A first step of evaluation was the implementation of the system architecture in a test chip which operates at typical power supply voltages of 5 V [89]. The system idea works at any power supply voltage higher than 1.2 V as discussed for the analogue components of chapter 2. All limitations that could occur at very low power supply voltages are bypassed with this prototype working at 5 V.

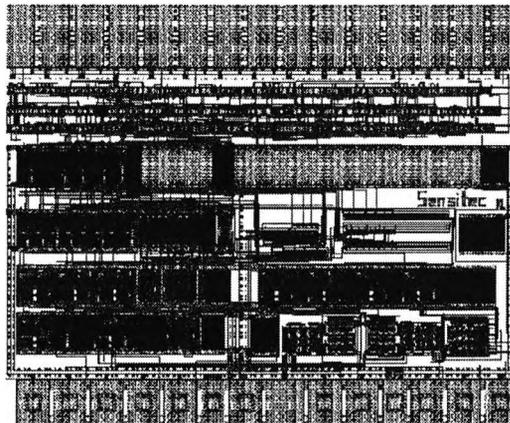


Figure 5.1: Chip photograph

The test chip includes instrumentation amplifiers at the input interface. They are able to operate with power supply voltages as low as 3.3 V. This is also valid for the analogue comparators. All bandwidth limitations of

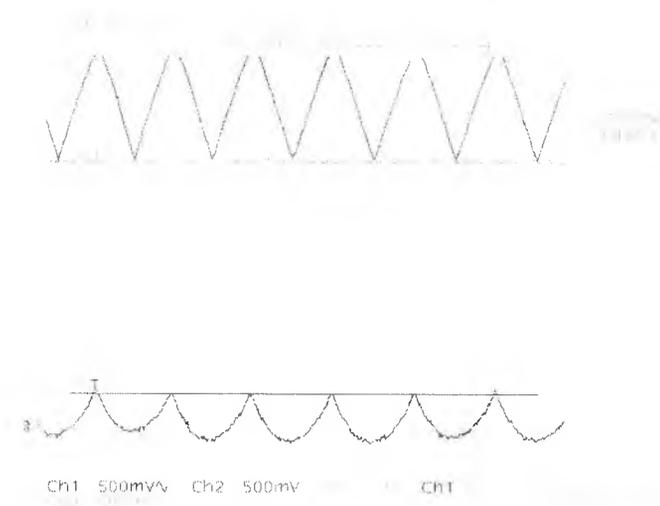


Figure 5.2: Measurement of the output of the folding unit

the components are much higher when compared with the components of section 2. This implementation has been done in a 0.7μ CMOS technology with a high resistive poly layer for linear integrated resistors. As a result a monolithic integration for the whole circuit was done for the analogue part (sec. 3) as well as for the digital encoder (sec. 3.4).

The chip photograph is shown in figure 5.1. At the top, digital pad cells for inputs and outputs are located. The encoder circuit is accommodated on the small rows below the digital core. A guard line separates the digital and the analogue part in order to reduce the substrate noise for the analogue part which is arranged below the digital circuitry. At the bottom analogue padcells are inserted for the sensor interface. Finally at the top, with the digital padcells, separate analogue power supply voltage pads are situated.

The test circuit contains various interpolation resolutions up to 20. That means the output frequency of the A and the B signal (sec. 3.4) is up to 20 times higher.

The test environment includes a rotating magnetic wheel, a magnetoresistive sensor element, the test chip and an oscilloscope. In order to observe the proper operation of the folding unit the voltages at the nodes V_{f1} and V_{f2} were measured. The result is shown in figure 5.2.

At the top the triangle like curve run of V_{f1} can be recognised. Its voltage at the lower vertex touches as expected, half of the power supply voltage. The wavelike curve run corresponds to V_{f2} and also behaves as expected.

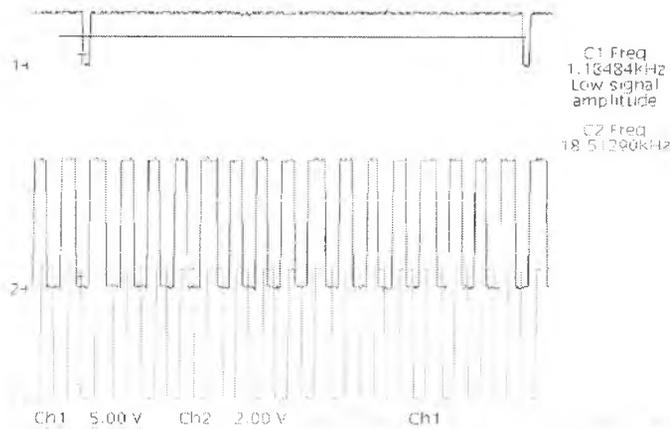


Figure 5.3: Measurement of the encoded output of the A/D converter

These voltages are linearized and interpolated by the flash converter with the nonlinear resistor ladder. For evaluation of the interpolation method an enhanced resolution of 20 was chosen. The test result is shown in figure 5.3.

The A/D conversion can be valued by observing the encoded output interface. The encoding circuit is fed by the temperature code of the A/D converter and delivers a two phase incremental output signal which can be recognised in figure 5.3 below the voltage V_{f1} . Concerning the accuracy, the differential nonlinearity error can be evaluated by measuring the distance from each edge of the digital signal to the next edge. For rating of the integral nonlinearity error each edge must be compared to the expected ideal position of the edge. Quantitative considerations of the errors are done within the next section 5.2.

All results of this section are related to the test of the hardware based algorithm for position measurement systems with enhanced resolution but without regarding low-voltage and low-power aspects. It can be concluded that the interpolation method operates properly. The following section evaluates the system behaviour at low-power and low-voltage conditions by simulation.

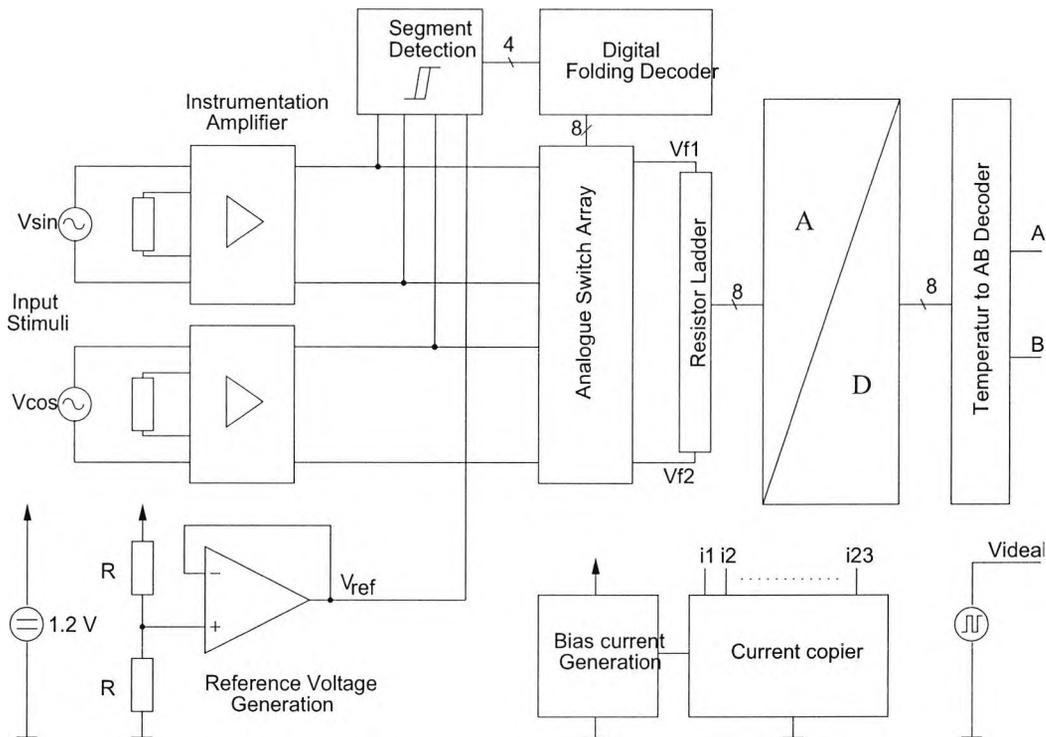


Figure 5.4: Testbench of the system

5.2 System Simulation Results

5.2.1 System Architecture

The system units and the interpolation methodology were introduced in section 3. With the low-voltage and low-power circuit cells of section 2 the circuit was simulated with a power supply voltage of 1.2 V. This is the minimum margin of operation.

Figure 5.4 shows the complete topology in a circuit diagram.

The instrumentation amplifier has been described in chapter 3.1.3. They amplify the signals of the sensor modeled by voltage sources. Mixed domain simulators allow the usage of the model introduced in section 4.1 instead of voltage sources. For the simulation an amplification of about 30 was adjusted. This corresponds to 100 k Ω and 7 k Ω , respectively, for the resistors R and R' of figure 3.3. The reference voltage V_{ref} of this figure is connected to the reference voltage generator of figure 5.4, which has an ideal value of $V_{DD}/2$ generated by the two resistors R .

Concerning the segment detection unit, four analogue comparators, as

accurately described in section 2.2.2, are included. The switching behaviour is described by the model equation 4.20. For controlling of the eight switches the folding decoder processes the outputs of the segment detection. Eight switches build a 4:2 analogue multiplexer for the four outputs of the amplifier and drive the two nodes V_{f1} and V_{f2} . Inside the A/D converter box, eight comparators are placed in order to generate at the output a thermometer code. Some EXOR gates and a logic for switching between an eighth period perform the encoding from the thermometer code to an AB-Signal at the output. The power supply voltage for the circuit is 1.2V.

Equations 3.19 and 3.20 have been taken for the calculation of the resistor string, where the total resistance R_{tot} was chosen as $1M\Omega$. As an example the resolution was set to 64. With an eight times folding the resolution of the A/D converter is 8. The nine required resistors and ideal phases are summerized in table 5.1.

k	$\varphi/^\circ$	$R_k/k\Omega$
1	2.81	46,826
2	8.44	82,348
3	14.06	71,137
4	19.69	63,206
5	25.31	57,580
6	30.94	53,660
7	36.56	51,076
8	42.19	49,605
9	-	524,571

Table 5.1: Ideal phases an the corresponding resistors values

The resistor values of table 5.1 were taken for simulation. On a layout level the resolution is limited by the grid and matching aspects, which depend on the technology. A lower accuracy of the resistors would be the result of higher resolutions. The corresponding error can be calculated by equation 4.12.

5.2.2 Benchmark Results

The capabilities of the system as described in the previous section 5.2.1 have been investigated. For comparision the system behaviour with ideal input signals has been tested. The internal errors which could not be idealized can be extracted, for example the systematic offset of the operational amplifiers

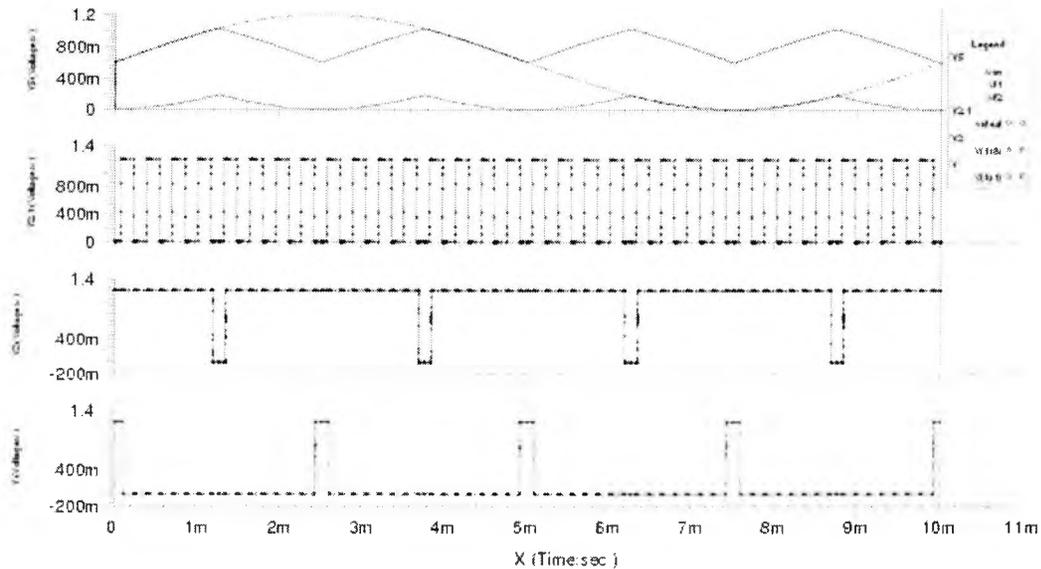


Figure 5.5: Simulation result of sensor system with ideal input signals

as well as the systematic offset and the hysteresis of the comparators. In addition the slight nonlinearity of the analogue switch in the region of $V_{DD}/2$, which has not been modeled, may play a part. The ideal sensor input signal has a low frequency of 100 Hz, an input amplitude of 10 mV and a DC-level of $V_{DD}/2 = 0.6 V$. For this signal frequency the phase shifts of the operational amplifier and the comparators are negligible. The chosen amplitude and the DC-level leads to output signals of the amplifiers very close to the power supply voltage. The following simulation results show the system behaviour.

In figure 5.5 four axes are stacked. The top axis shows the folded signals V_{f1} and V_{f2} as well as a sine waveform. It can be observed where the folding signal is a part of the sine. Obviously the folding signal is not distorted visibly by the analogue switch. The amplified sine and cosine waveforms have amplitudes of $V_{DD} - 10 mV$ or $V_{SS} + 10 mV$, respectively. On the axis below for comparison an additional ideal rectangle waveform generated by a voltage source is shown. Each expected switching point of the comparator chain can be compared with the real one as shown on the last two axes. The output voltage of the first and the last comparator of the A/D converter is shown. The width of the pulses imply the differential error at the location between two neighbouring folding units. Recalling the results of the error model, the largest error appears at this location. In detail the measured values are depicted in figure 5.6.

The values on the axis of ordinates were calculated by $DNL = (te_k -$

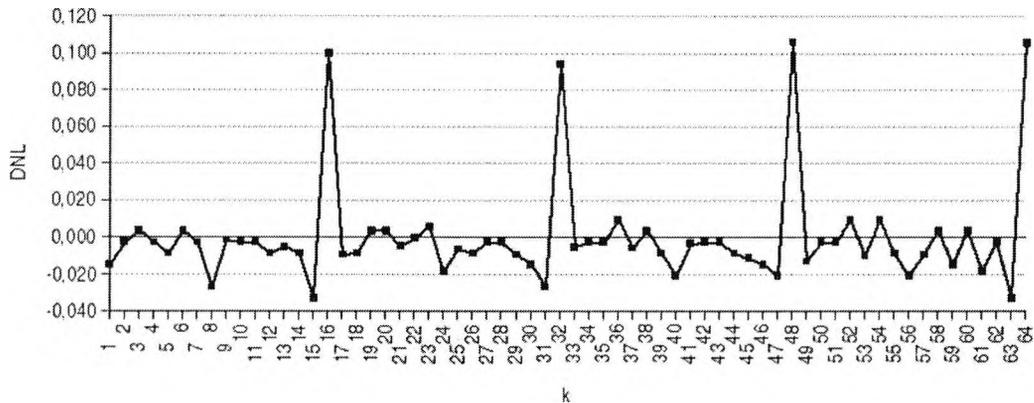


Figure 5.6: DNL with ideal input signals

$te_{k-1}/LSB - 1$, where te represents the time where the edge occurs, k is the number of the edge and LSB is the smallest ideal increment. Some internal errors exist which limit the achievable accuracy. This result is the best case result. It would be worse for a real system because stochastic errors such as offset and resistor mismatch exist. In addition the errors caused by non ideal input signals increase the error if these errors are not compensated. Offset errors can be compensated externally but amplitude errors and signal distortion is normally not corrigible.

The systematic internal errors in terms of the INL are depicted in figure 5.7. Also the INL error shows discontinuities at the location of folding. The error seems to be folded, too.

One remark should be made concerning the evaluation of the system errors. Typically the transfer curve of an A/D converter is corrected before specifying DNL and INL. Offset and gain errors are previously compensated. That means these errors are normally not considered. But these results include both errors and contains therefore the overall error. The INL error indicates a systematic error because integral errors are expected to be zero at the beginning and at the end.

Table 5.2 contains the simulation results with respect to the power consumption.

For the complete circuit 9 OPAMPs and 12 comparators have been used. Calculating the overall current from the number of components and the simulated currents of both components leads to the result, that only these components contribute, as expected, significantly to the total power consumption. The same results have been achieved for signals with smaller amplitudes.

Smaller amplitudes influence the accuracy of the signal processing. As

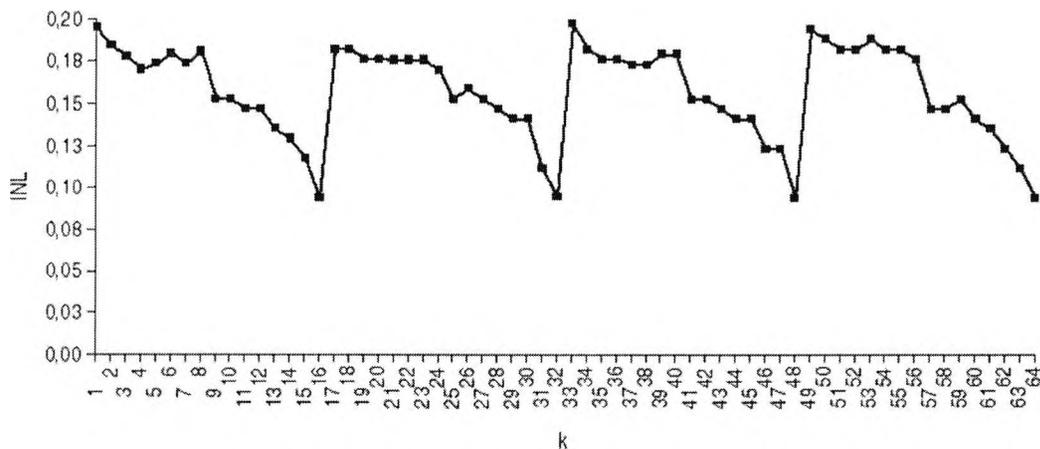


Figure 5.7: INL with ideal input signals

Parameter	Symbol	Value	Unit	Note
Power supply voltage	V_{DD}	1.2	V	
Supply current	I_{DD}	216	μA	average
Power consumption	P_{tot}	259	μW	average
Comparator current	$I_{DD,comp}$	4.2	μA	average
OPAMP current	$I_{DD,op}$	18.5	μA	average, loaded

Table 5.2: Simulation results of the system

described in chapter 3.2 the signal processing method is approximately amplitude independent. But for smaller power supply voltages the dynamic range is reduced and the internal errors become more serious.

The following example includes only two errors. First, the offset of the A/D converter comparators $V_{off,comp}$ alternates by ± 5 mV and the internal hysteresis of the comparators V_{hys} is 3.2 mV. The DNL error for amplitudes of the amplified input signals have been swept by 400 mV (DNL4), 500 mV (DNL5) and 600 mV (DNL6). The result is depicted in figure 5.8.

As expected the differential nonlinearity decreases with increasing amplitudes. The error alternates around zero. For this error and the maximum possible amplitude, the error cannot be smaller than 25 %. For higher power supply voltages or smaller offset values a better result can be achieved. Nevertheless the system operates properly also for smaller amplitudes. That means all 64 edges appear within the period.

Regarding the position related error an INL error analysis has been done.

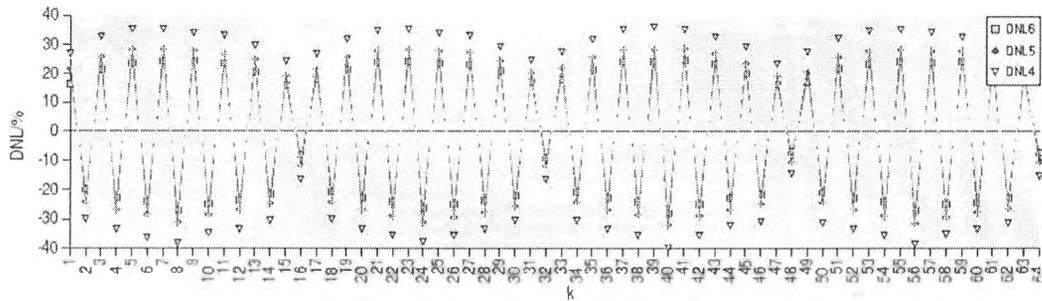


Figure 5.8: DNL for different amplitudes

For the above given example the INL error is shown in figure 5.9.

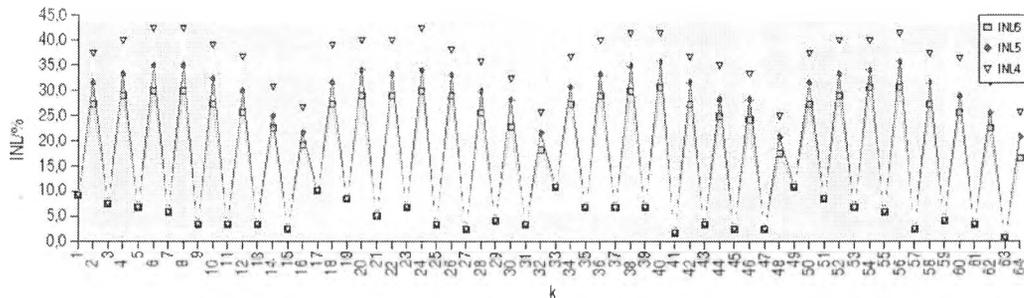


Figure 5.9: INL for different amplitudes

The maximum deviation from the ideal position of some edges are about 40 % if the amplitude is 400 mV (INL4). For these small amplitude the offset of the comparators have a large influence. Furthermore the discontinuities between the folding point can be observed.

Figure 5.10 shows a simulation result which can be taken as an example for all preceding analyses. The top axis shows all amplified sensor element signals as well as the transformed signal of the folding unit. On the axis below a separate generated output signal indicates the ideal position for each edge within the period. Comparing each edge on the two last axes with the ideal signal leads to the INL error. If the A- and the B-signal on the last two axes are combined by an extra XOR gate, the DNL error can easily be extracted. It can be noticed that the cycle width, the duty cycle and the phase shift between A and B changes within the period. The same pattern of error repeats in each period if the errors do not change. Such a result is very often within the required accuracy of position measurement systems.

In figure 5.11 a similar simulation result is shown. The main difference

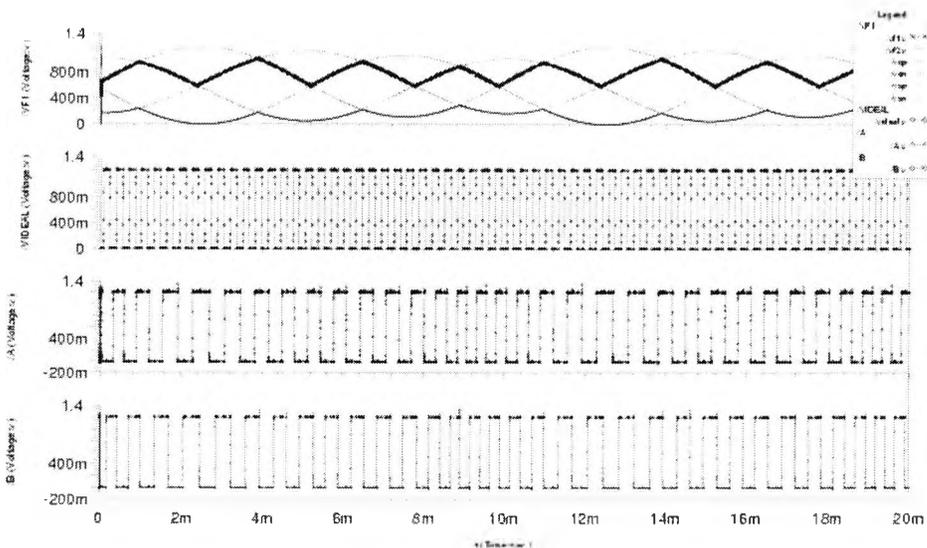


Figure 5.10: Simulation result with input errors

is that the voltage curves of the first axis clip at the negative power supply voltage due to too high input signal amplitudes. This generates distortion. The method is fault-tolerant but an increase of the DNL and INL error will be the result.

5.3 Discussion

5.3.1 Chain of Evidence

Several steps of investigation have been accomplished where three main parts have been discussed. First, the chapters 2.1.1, 2.1.2 and 4 include models on a component and system level, respectively. Based on the knowledge of the component and system behaviour theoretical limits can be determined. Second, simulation results on a component and system level show the operation of the new method. Third, measurements have been done on a component level as well as on a system level.

Basically on a component level, measurements have been done on component rudiments. Measurement and simulation results are demonstrably in congruence. The margins of operation have been determined first by model equations. Therefore large and small signal behaviour as simulated for the optimised and adapted components can be extrapolated and it can be demonstrated that the components operate as expected.

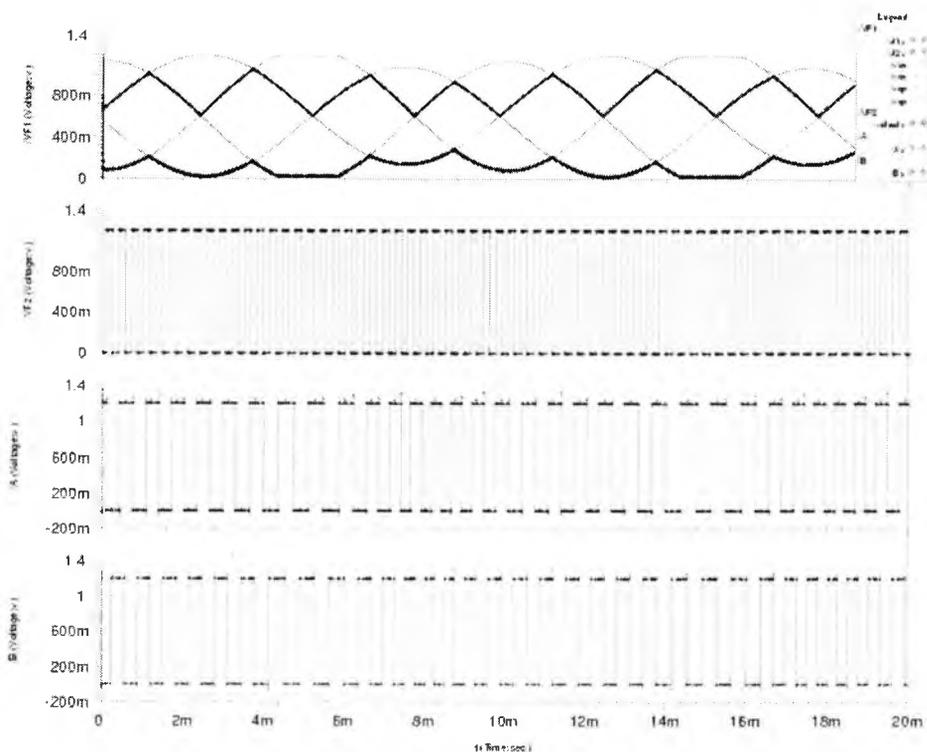


Figure 5.11: Simulation result with saturated output signals

On a system level the proper operation of the new method has been shown by measurements at a power supply voltage of 5 V. The model behaviour, measurement and simulation results are consistent. Based on the verification on a component level the correct operation of the interpolation method at power supply voltages of 1.2 V has been furnished by proof by simulation.

5.3.2 Component Level

The analogue components determine the performance of the position measurement system. The effect of the digital components can be neglected in respect of all vital parameters.

As discussed in section 2.2.2 each comparator contributes to the power consumption of approximately $5\mu\text{W}$ at $V_{DD}=1.2\text{ V}$. Regarding the power supply voltage the comparator is limited by its rail-to-rail input stage. This problem cannot be bypassed for the comparators of the folding unit because two of the comparators compare sine and cosine. For maximum amplitudes of 0.6 V the crossing points are at $0.6\text{ V}/\sqrt{2} = 0.42\text{ V}$. Hence the common

mode input range has been up to within 180 mV of the power supply voltages.

The comparators of the A/D converter have a fixed reference of $V_{DD}/2 \approx 0.6$ V. A rail-to-rail input stage is therefore not necessary. The rail-to-rail input stage ensures a steady current through the input stage. On the one hand this might be an advantage in respect of the recovery time of the current sources if the input voltages push the current sources out of saturation. But on the other hand a lower power consumption would be the result if a single input stage is used.

The performance of the comparator is sufficient in terms of propagation delay time as well as rise and fall time. The offset of the comparator influences significantly the precision as discussed in this chapter. Therefore a careful handling on the architectural and physical design level is necessary because a manual offset compensation for the comparators is not possible.

Concerning the hysteresis of the comparators the level of $V_{hys} \approx 3.2$ mV is sufficient in respect of the switching noise which has been determined by simulation. The noise of components is also smaller than the hysteresis. If the sensor system is used in harsh environments this hysteresis might be too small. Such external effects are not covered by this work.

The input stage of the OPAMP limits the input stage of the comparator as well as the minimum possible power supply voltage. For the specified technology the minimum power supply voltage is 1.2 V. Due to the implemented rail-to-rail input and output stages signal processing is possible over the complete power supply voltage range. There is no further limit given by the OPAMP itself.

With a power consumption of ≈ 22 μ W (table 5.2) the OPAMP including load is the most significant component of the system in terms of power consumption. Within the example of this chapter all nine amplifiers consume more than 77 % of the total power for an interpolation value of 64. The ratio becomes better for higher interpolation values where more comparators are needed. But nevertheless the amplifier will be the limiting factor.

Furthermore the operational amplifier limits the system performance with respect to the signal processing speed. The gain bandwidth product GBP of ≈ 500 kHz limits the input frequency to about 10 kHz to 20 kHz depending on the required amplification. For a typical period of a magnetoresistive sensor element of 1 mm this equals to a speed of approximately 10 m/s for position measurements. This is absolutely sufficient for most applications.

As shown in section 5.2.2 the ratio of the offset to the amplitude determines significantly the accuracy of the system. Therefore a low offset of the amplifiers are required. On an architectural level, large input transistors as well as large load transistors of the amplifier have been chosen in order to minimise the offset. Often the overall offset of the sensor element and the

electronic circuit is externally compensated. Then this influence can be neglected. This is different to the comparator where no external compensation is feasible.

The analogue switch limits also the minimum possible power supply voltage as discussed in section 2.4. It is a critical component, because the analogue switch can contribute to signal distortion. Only if the current through the transmission gate is small and in addition if the bulk of the p-channel transistor is biased will the required linearity be obtained. Moreover the switch causes charge injection. If these voltage transients are too large in respect of the hysteresis of the comparator, output chatter could be the result. In order to prevent this dummy transistors inside the analogue switch have been used in order to compensate this effect. The power consumption of the transmission gate is negligible.

Apart from the analogue components the digital cells have been developed and proved at low power supply voltages (see section 2.5). The usage of digital cells at 1.2 V power supply voltage is uncritical. For alternative technologies the minimum power supply might be different but the limit is always given by the analogue components and not by the digital gates.

5.3.3 System Level

The signal conditioning methodology has been discussed in chapter 3.2 and evaluated in this chapter. The method can be divided into two parts. It transforms and linearises the analogue input signal. An enhanced resolution is achieved by interpolation of the input signal.

Linearisation of the input signal is obtained within the A/D converter. From the viewpoint of power consumption no additional power consumption must be spent for linearisation, because an A/D converter is needed in any case. Hence the linearisation method is well suited for low power applications.

All matching problems which are related to the resistor string are basically given by all resistor based A/D converters. High resistances lower the power consumption but enlarge on the other hand the required chip area. Concerning the reduced power supply voltages, accuracy requirements of the resistor string become more serious. This can be evaluated by inspection of the DNL error. Large areas of such resistors on the die lower this type of error. This error is superimposed by the offset error of the comparator, the hysteresis, and the offset voltage of the reference voltage. A detailed investigation of the error can be done by applying the model (sec. 4.2.2) of the system architecture or by simulation.

The resolution can be increased by increasing the number of sampling nodes of the A/D converter. In contrast to conventional A/D converters no

binary weighted range is necessary. The achievable resolution within one octant only depends on the precision of the components and elements. As explained in section 5.2.2 and depicted in figure 5.6 the internal errors limit the DNL error to a minimum of $\approx 3\%$ if the errors at the folding points are neglected here.

This interpolation method can also be applied if no additional signal folding is done. For example the range for the resistor string can be enhanced up to a quarter or a half of the period.

One further advantage of this linearisation method is that the voltages V_{f1} and V_{f2} are subtracted across the nonlinear voltage divider of the resistor string. Both signals are processed at the same time. If this would be done separately by two A/D converters the number of comparators as well as the power consumption and the die area are doubled. Furthermore this concurrent signal processing method suppresses common mode disturbances. If two conventional flash A/D converters were to be used instead, it would be possible that common mode disturbances and voltage transients could be measured at different sample times due to signal delays. A compensation could only be done by much more effort of digital computation.

Regarding the dynamic range, this method provides a fixed dynamic range without loss. Typical for conventional conversion methods is that the amplitude of the signal is smaller than the reference voltage. If, for instance, the amplitude is halved the resolution of the converter is also halved - in contrast to the proposed method. The signals themselves determine the dynamic range. As a result the resolution is never reduced. In low voltage designs any further loss of the dynamic range is absolutely undesired.

The second part of the signal conditioning method is the folding unit. The advance in respect of power consumption reduction is obvious. To achieve the same resolution without folding the number of comparators have to increase. Depending on the applied method of conversion, the improvement can be up to eight times lower power consumption and chip area of the A/D converter. The multiple usage of one and the same A/D converter makes this possible. Based on the symmetry of the input signals the smallest possible signal folding is $N_f=8$. Compared with other folding techniques as used for A/D converters, this method is different. It transforms the signal at the input itself.

As exposed by the calculation results, of the model and the simulation results the DNL and INL error increases at these folding point. The reason can be voltage steps of the voltages V_{f1} and V_{f2} . If only V_{f1} is folded and not V_{f2} at this phase or time, respectively, the error becomes significant. If both signals are switched this inaccuracy is similar to a common mode step and is therefore suppressed. This problem is only obvious if no other error

superimposes this error. As a result of figure 5.6 this error limits the smallest accuracy possible for the system. The DNL error is here about 10 %.

It can be concluded that the major limitation of the system architecture is given by the offset error of the comparator. This is depicted in figure 5.8. If an offset of ± 5 mV is assumed the DNL is between 20 % and 35 % and therefore larger than the error caused by the signal folding. From this diagram and the INL error in figure 5.9 it can be noticed that the error curves for amplitudes of 600 mV and 500 mV are close together. In other words, the amplitude dependency is only slight and negligible. Within this range the signal processing is approximately amplitude independent.

5.3.4 Implementation

The proposed method has been proved in a $0.5 \mu\text{m}$ CMOS technology. The most interesting parameter with respect to the minimum possible power supply voltage is the threshold voltage of the transistors. They are 0.6 V for both, the n-channel and the p-channel devices. As a result of this limiting condition the power supply voltage could not shrink below 1.2 V. For other technologies the minimum margin can be either higher or smaller.

If the circuit is implemented in a $0.5 \mu\text{m}$ CMOS technology the chip area can be estimated. For the example of this chapter the resolution is 64. Table 5.3 summarises the required areas of the components based on the layouts which have been developed for the rudimentary comparator and OPAMP.

Component	Area/ μm^2	Number	Total Area/ mm^2	Note
OPAMP	500 · 140	9	0.630	
Comparator	300 · 140	12	0.504	
Bias Circuit	400 · 140	1	0.056	incl. resistors
Current copier	200 · 140	1	0.028	
Analogue Switch	20 · 140	8	0.022	
Resistors of amplifiers	200 · 200	2	0.08	
Resistor VDD/2	350 · 150	1	0.053	
Resistor ladder	350 · 120	1	0.042	$5 \mu\text{m}$ width
Digital components	200 · 25	1	0.005	
Pads	320 · 150	10	0.48	
Total		46	1.9	

Table 5.3: Estimation of the required chip area

As concluded in table 5.3, the total die area approximately 2 mm^2 . Not included are wire channels and power lines. They would increase the die

area slightly. OPAMP, comparator and pad cells are area dominant and consume more than 80 % of the total die area. Ten pad cells are necessary as a minimum for the input interface of four sensor element terminals and a further four padcells for two separate power supplies for the analogue and digital part. The output interface requires two pad cells for the A and B output signals.

5.3.5 Optimisation Prospect

On a system level, the best solution possible has been found with respect to the reduction of the number of components. Due to the signal symmetry of the two input signals the A/D conversion has been adapted for this special case. The major benefit is the significant reduction of components and thus of power consumption especially for high resolutions.

But in respect of accuracy and performance further investigations can be done based on the results of this work. Obviously the major influence of the accuracy is the ratio of the amplitude to offset. Both, the OPAMP and also the comparators contribute to this inaccuracy. Large device dimensions of the input stages of these components have been used in order to keep the offset as small as possible. For smaller offsets switched capacitor (SC) techniques must be used. This kind of signal processing is different to the proposed type of signal processing and needs a system clock which must be generated by an additional oscillator. This would increase the power consumption. This might be a solution if the oscillator circuit, the SC-OPAMP and the SC-comparator do not consume much more power. One major drawback of SC techniques is the noise of the switching components. Therefore it is important that the additional noise does not undo the benefit of offset compensation. Particularly at low power supply voltages the switching noise could limit the accuracy of the system.

The input amplifier is an instrumentation amplifier which consists of three OPAMPs. A further OPAMP is used for regenerating the inverted sine and cosine phases. An optimisation in terms of power consumption and phase shifts between input and output signal might be a fully differential amplifier. A fully differential amplifier would combine two OPAMPs. Also in terms of rejection of common mode signals this could be an advantage. Fully differential amplifiers consist typically of a differential input stage and of a common mode feedback circuit. The feedback circuit also consumes power. Therefore it could be that the advantage is small or that no advantage exists. The proposed instrumentation amplifier is a good base for evaluating if such a fully differential amplifier could decrease the power consumption.

One topic has not been covered by this work. On a system level bandgap

circuits supply the whole circuit with a power supply and temperature independent reference voltage. The reference voltage as described in section 2.3.4.1 provides only a power supply independent reference voltage. An extension of this circuit to include a temperature compensation is not possible with traditional concepts because obviously the reference voltage is larger than the power supply voltage of the system. As a result new concepts are necessary. One possible solution has been proposed by Malcovati [79]. Hence it is feasible to operate with smaller temperature compensated reference voltages such as 1.25 V. This advance is not a condition for this work.

5.3.6 Classification

Various position measurements have been realized and are available in the market place. In order to compare this work with a sample of these other designs, datasheets from different commercial products have been evaluated [80], [81], [83], [84], [85], [90]. Table 5.4 includes a technical summary of these products.

Product	VDD _{min} /V	P / mW	Interpolation Method	Max. Resolution
UZZ9000	4.5	65	digital	1000
IP200	4.75	166	digital	200
IP501	4.75	403.8	digital	500
STINT	3.6	35	analogue	80
IC-NG	4.5	112.5	analogue	256
IC-NV	4.5	90	analogue	64
This work	1.2	0.26	analogue	64

Table 5.4: Summary of commercial available IC's for position measurement

It has, however, been very difficult to make any accurate comparisons between the various commercial products, or between them and this design. Each of the commercial designs contain certain elements of the sensor interface (e.g. input amplifier, A/D converter, linearization circuitry, offset compensation techniques, gain control, etc.) and will have been optimized for speed, accuracy, cost, power consumption, etc.

Since this design has been concerned with the minimization of power consumption and operating voltage, it has been compared on this basis. In order to make the comparison as meaningful as possible, it was decided to

normalize the manufacturers figures to a power consumption per "bit". The results are shown in figure 5.12.

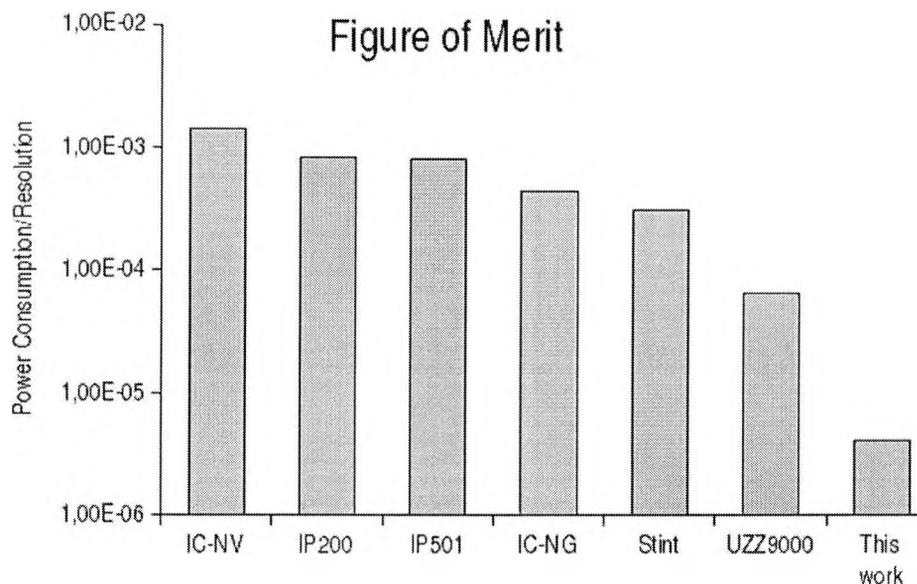


Figure 5.12: Figure of merit

The advance by saving components and operating at smaller bias currents is obvious from figure 5.12. All of the commercial designs are operating in addition at power supply voltages of larger than 4.5 V, except for the STINT design (3.6 V). The resolution values range from 64 to 1000.

This design consumes 16 to 350 times less power than the compared systems. As previously explained, the performances are not completely comparable because the system architectures differ significantly for some of the designs. Nevertheless, it can be seen that this approach needs much less power per "bit" than all other systems.

Chapter 6

Conclusion

With new concepts for the circuit and the system, this work achieves a power supply voltage as low as 1.2 V for AMR position sensor applications. Vital components like operational amplifiers and comparators were designed to operate at this small supply voltage with very low currents.

Based on the chosen technology (0.5 μ CMOS process) the margin of the supply voltage is as low as it can be. In conjunction with a magneto resistive sensor the integrated circuit processes at the analogue interface sine and cosine sensor signals at supply voltages that are only limited by the electronic circuit. Both sensor and integrated circuit can be supplied with a single supply voltage by conventional batteries for years, where no extra sleep and wake up mode for the circuit is implemented. The system operates continuously in the time domain and consumes several μ W depending on the resolution and number of components, respectively. The sensor itself contributes a consumption of approximately some ten μ W, depending on the sensor type. In previous sensor solutions the power consumption of the sensor compared with the circuit was so small that it could be neglected. With this new integrated circuit principle the sensor influence with respect to power consumption is no longer insignificant. Compared with other systems this system only needs a fraction of the total power consumption. The overall goal of a significant power consumption reduction is therefore achieved with this approach.

Several steps were necessary to obtain such small power consumptions. On a circuit level the electronic elements are mostly driven in the weak or moderate inversion region and for that reason the currents of the electronic components become very small. One result is that at a component level, basic cells were developed that are able to operate at such small currents. The bias currents for parts of a component were chosen in a range of 10 nA to 500 nA, so that the transistors were biased in the weak inversion region. A further

advantage is facilitated along with the weak inversion operation of the MOS transistors. Almost all important voltages such as the gate-source voltage and the drain-source voltage can shrink and hence the minimum supply voltage decreases. That also has a positive effect on the power consumption of the sensor. This is of interest, if the power consumption of the sensor elements also drops with smaller power supply voltages. Both, circuit and sensor element have the same power supply voltage.

On a system level, this approach is distinguished from all other known methodologies for enhanced resolutions of position measurement systems by an ADC architecture which folds the input signal and linearizes them. Moreover, this conversion topology deals with a concurrent signal processing of two input signals. Neither a second ADC nor an additional analogue multiplexer circuit is necessary yielding a significant power consumption saving. Furthermore the two input signals determine the dynamic range of the ADC, whereas traditional concepts have a fixed reference voltage. For these types of conversion the resolution is smaller if the signal voltage range is smaller than the voltage range. In addition, the period of the input signals can be separated into eight parts. Consequently the A/D conversion of the input signals can be done with a new folding design which reduces the number of comparators and resistors by a factor of eight if the symmetry of the sensor signals is taken into account. For high resolutions this provides a significant improvement in power consumption and chip area.

Furthermore, the A/D converter includes the linearization of the sensor signals. A new nonlinear resistor network inside the converter fits the input to ideal sensor signals. Therefore, a new model is proposed for the nonlinear and folded ADC in order to investigate the topology and signal errors. With this fully parametric model the maximum interpolation value can be determined, which, for instance, depends on matching errors of the resistors or the component offsets.

This study's findings can be transferred to other applications, than position measurement systems. Low voltage and low power aspects are of interest in a lot of developments, particularly if the requirements of speed are low it is not necessary to apply traditional integrated circuit concepts within low power and low voltage environments. The design of circuits at the margin of transistor operation can improve the power supply voltage range of circuits and systems as well as reduce the total power consumption.

In addition the new concept of the flash ADC can also be transferred to other applications. If the sensor element provides two phase shifted and periodically signals of any waveform e.g. triangle it is possible to use the dynamic related reference concept in order to improve the signal to noise ratio. For nonlinear input signals the linearization can be done within the

ADC and so it is possible to dispense with software algorithms or digital linearization. The advantage is that the linearization does not generate extra effort in signal processing or extra circuitry.

The future potential for the work is considerable. The overall architecture was proven in the form of a test integrated circuit and a commercial design, utilizing the interpolation method, is now in full scale production, for use in vehicle braking systems. This commercial product operates at a power supply of 5V. In addition, the design is being used in several motor encoders for angle measurement and for a wide variety of length measurement systems, like sawing machines.

The ability of the design to operate down to a supply voltage as low as 1.2V will open up other potential markets, some of which have not hitherto been feasible with more traditional methods.

A patent application has been submitted for the method of resolution enhancement [96] and a decision is expected in the near future.

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