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A Phase Error Correction System for Bioimpedance Measurement Circuits

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Abstract: Bioimpedance sensing is widely used across a spectrum of biomedical applications. Among the different system architectures for measuring tissue impedance, synchronous detection or demodulation (SD) stands out for its lock-in amplifier utilising in-phase (I) and quadrature (Q) demodulation signals to derive real and imaginary impedance components. Typically, the current injected into the tissue is controlled by a voltage-controlled current source (VCCS). However, the VCCS can introduce phase shifts leading to discrepancies in real/imaginary outputs, especially at the highest end of the operating frequency bandwidth. Such discrepancies can significantly impact diagnostic accuracy in applications reliant on precise tissue phase profiling, such as cancer and neuromuscular evaluations. In the present work, we propose an automatic phase error compensation stage for bioimpedance measurement systems to minimise this systematic error. Our experimental findings demonstrated a considerable reduction in phase error, with the Phase Error Compensated Synchronous Detection (PECSD) system exhibiting a maximum phase error of 2° (≤5% error) compared with the uncompensated SD system where error exceeded 20%. The improvements made by our proposed SD system hold great potential for enhancing the accuracy of impedance measurements, particularly in clinical diagnosis and disease detection.

Keywords: bioelectrical impedance; bioimpedance; synchronous demodulation; synchronous detection; phase error; PECSD; electrical impedance; electrical impedance spectroscopy

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1. Introduction

Bioelectrical impedance or bioimpedance sensing, a versatile sensing method widely employed in diverse biomedical applications, plays a pivotal role in detecting pathologies, monitoring physiological processes, and assessing tissue dynamics. It has been applied to a range of critical areas, such as evaluating skin hydration [1], differentiating between healthy and cancerous tissue [2], evaluating heart and lung function [3], and detecting tissue ischemia. Additionally, it facilitates comprehensive analyses of body composition, imaging of various anatomical regions, and monitoring wound healing [4]. Moreover, bioimpedance also serves as a valuable tool for assessing muscle health in neuromuscular diseases [5].

Bioimpedance measurement systems feature an output stage applying an AC voltage or current to biological tissue and an input stage measuring the resulting current or voltage, thus allowing impedance to be calculated. Although the output stage is often designed to be voltage-generating due to simpler associated circuit architectures, current output stages are considered safer in terms of minimising the risk of tissue damage and compliance with medical safety standards [6,7].

When it comes to the measurement stage, various architectures can be employed, with synchronous demodulation (SD), magnitude and phase (MP), or synchronous sampling (SS) circuits commonly employed in true tetrapolar configurations. Meanwhile, bridge and oscillation-based feedback topologies are the most prevalent in bipolar or pseudo-tetrapolar

configurations [7–9]. Among these, SD architecture is the most widely employed, especially for multifrequency tetrapolar measurements, featuring four electrodes to overcome electrode contact impedance-related errors. It uses both an in-phase (I) and quadrature (Q) signal for demodulation, generated with a 0° and 90° phase shift relative to the applied signal, enabling the extraction of the real and imaginary components of impedance, respectively. SD systems can measure very weak signals without supplementary bandpass filters owing to their lock-in amplifier mechanism [6,10].

Research on improving SD-based systems predominantly focuses on minimising systematic errors that affect the measured impedance magnitude, including bandwidth limitations and issues related to output current amplitude degradation at frequencies higher than 100 kHz [6,10]. Minimal research and attention have been devoted to rectifying inaccuracies in SD phase detection stemming from nonidealities on the signal generation side, causing the voltage-controlled current source to introduce phase shifts, altering the synchronization of the injected current with the in-phase (I), and quadrature (Q) demodulation signals. Although less detrimental than the current injection due to I,Q phase errors, further phase shifts can be introduced by preamplification stages on the monitoring side of the system. The injected signal, I,Q phase errors, result in frequency-dependent measurement degradation, which reduce the suitability of conventional SD systems for bioimpedance-sensing applications where precise phase detection is critical for accurate disease diagnosis, including assessment of cell integrity, cancer detection and characterisation, and myography [2,11].

To the best of the authors' knowledge, most previous studies towards improving the phase accuracy of measurements in SD systems focused on ASIC realizations. When it comes to commercial realizations, Texas Instruments (TI) (Dallas, TX, USA) offers AFE4300, a specialised integrated bioimpedance circuit based on SD topology primarily designed for body composition analysis and weight scale applications. However, it has constraints regarding load and bandwidth. It can handle maximum reactive and resistive loads of 700 Ω and 22 Ω, respectively, and its bandwidth is limited to ≤80 kHz [12,13]. Analog Devices (ADs) (Wilmington, MA, USA) offer MAX30001-MAX3002, both SD-based bioimpedance instrumentation ASICs, which deliver performance comparable to standard laboratory impedance analysers. However, they can only achieve a maximum bandwidth of 131 kHz [12,14]. MAX30009, another AD solution, is their latest and most accurate SD-integrated solution. However, to obtain the level of accuracy claimed in the datasheet, phase errors must be calculated for each stimulus frequency, making it unsuitable for impedance spectroscopy applications [15]. A CMOS ASIC research realization presented in [10], co-authored in part by members of our team, featured the approach of passing I and Q demodulation signals through the same preamplification stages as the first stage of the monitoring sub-system to minimise relevant phase errors. However, whilst this approach worked, it only achieved <4% error for RC loads at frequencies up to 100 kHz. Phase errors were identified as a serious issue affecting bioimpedance measurement accuracy in [16], which focused solely on a CMOS phase shifter simulation. The theoretical paper did not demonstrate how they would integrate with a bioimpedance measurement system nor did it identify how phase error would be identified prior to compensating for it.

The present work introduces a Phase Error Compensated Synchronous Demodulation system (PECSD), an SD-based bioimpedance measurement system with automatic phase error correction that can achieve less than 5% phase errors for RC loads for frequencies up to 300 kHz. The topology presented here achieves minimal error at reasonably higher frequencies and does not require recalibration for each phase unlike other implementations, including ASIC-based ones.

Figure 1 illustrates an equivalent circuit for human skin impedance. It provides a structured display of tissue layers and their interaction with bioimpedance measurement systems and instrumentation (Figure 2) using a tetrapolar electrode configuration. Figure 1 also illustrates an unwanted element: the introduction of erroneous phase shifts by instrumentation, compromising results accuracy. Most bioimpedance applications that depend on phase shifts

between injected and measured signals for accurate diagnostics are predominantly performed at relatively high frequencies, i.e., skin cancer and impedance myography [2,17,18]. Most injected current paths traverse through the membrane/capacitive layer.

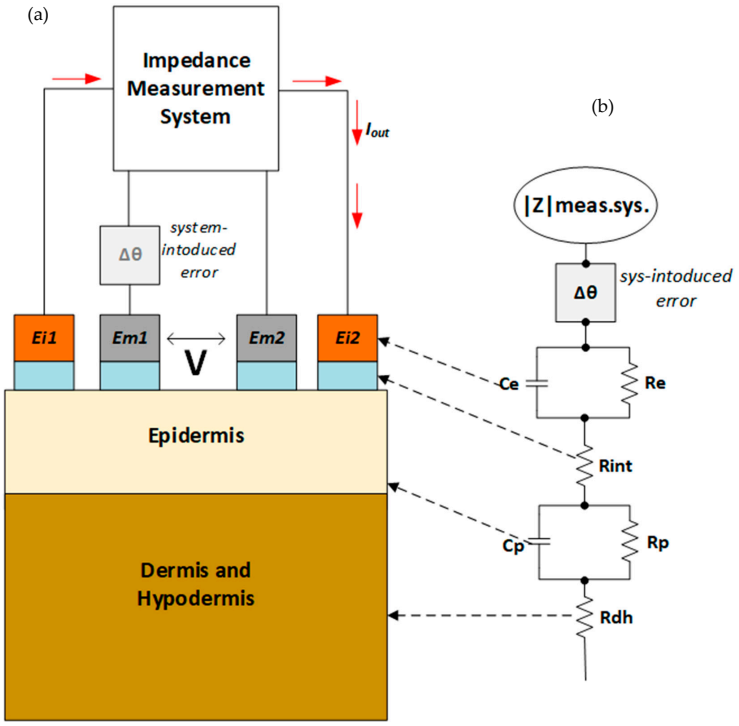

Figure 1. Equivalent circuit of human skin impedance showing (**a**) the system-introduced phase error on skin tissue and (**b**) the equivalent circuit model of one channel of (**a**), identifying the tissue's layered structural circuit components. Ce and Re are associated with the electrode/electrolyte interface. Rint represents interface effects due to the electrolyte. Cp and Rp are parallel RC circuits of the epidermis, while Rdh represents the dermis and inner layers [16,19].

Consequently, any additional phase shifts introduced by the measurement systems contribute to overall phase shifts in the membrane capacitance. This dual-phase shift scenario presents challenges: users cannot discern the extent of erroneous phase shifts versus those originating from the tissue itself [20]. Moreover, manually correcting these errors becomes arduous due to their frequency dependency. Each swept frequency results in a different phase error. Addressing these challenges is pivotal to enhancing the accuracy and reliability of bioimpedance measurements.

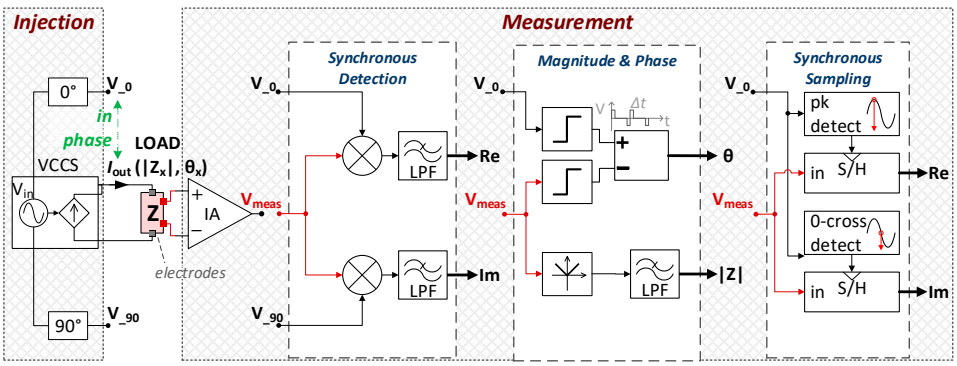

Figure 2. Bioimpedance measurement topologies based on Synchronous Detection/Demodulation (SD), Magnitude and phase (MP), and Synchronous Sampling (SS). Ideally, V_{in} (and $V_{\_0}$) are in-phase with the injected current I_{out} [21–25].

2. Methods

2.1. Phase Error Analysis

As earlier stated, bioimpedance involves the injection of low-amplitude alternating current $i_{out} = i_o \sin(\omega t)$ into the biological tissue, where i_o = the amplitude of the injected constant current from the current source. Measured voltage v_{meas} relative to the reference voltage V_{in} and affected by the erroneous phase shifts of the VCCS can be expressed as:

$$v_{meas} = A_v i_0 z_x \sin(\omega t - \varphi - \Delta\theta) \tag{1}$$

where, A_v is the gain of the measuring instrumentation amplifier; $|Z_x|$ is the measured impedance magnitude determined by applying Ohm's Law to the relationship between the measured voltage and the injected current as in Equation (1); $\angle Z_x$ is the measured impedance phase; φ = tissue impedance phase (ideally equal to $\angle Z_x$); $\Delta\theta$ = erroneous phase due to frequency dependent delay by VCCS.

Demodulation signals were used to further extract impedance data from v_{meas}, including in-phase lock in signals (v_0) and the quadrature sinusoidal signal v_90, defined as:

$$v\_0 = v_0 \sin(\omega t) \tag{2}$$

$$v\_90 = v_0 \sin(\omega t + 90^\circ) \tag{3}$$

The in-phase demodulation procedure involves multiplying v_{meas} by v_0, yielding the output of the in-phase multiplier:

$$v_{mult0deg} = \frac{A_v i_0 Z_x v_0}{2}[\cos(\varphi + \Delta\theta) - \cos(2\omega t - \varphi - \Delta\theta)] \tag{4}$$

The output of the multiplier $v_{mult0deg}$ is also passed through a low-pass filter to eliminate high-frequency components, leaving out the DC components. The output of the low pass filter for the in-phase demodulation is:

$$v_{LPF0deg} \approx \frac{A_v i_0 Z_x v_0 (cos\,(\varphi + \Delta\theta))}{2} \tag{5}$$

Hence, the real part of the impedance is:

$$Re = (cos(\,\varphi + \Delta\theta)) = \frac{2 * v_{LPF0deg}}{A_v i_0 v_0} \tag{6}$$

Similarly, the quadrature demodulation procedure involves multiplying v_{meas} by v_90, yielding the output of the quadrature multiplier (v_{mult90°).

$$v_{mult90^\circ} = \frac{A_v i_0 Z_x v_0}{2} * sin(2\omega t) * \cos(\varphi + \Delta\theta) - \frac{A_v i_0 Z_x v_0}{2} * cos(2\omega t) * sin(\varphi + \Delta\theta) \tag{7}$$

v_{mult90° is also passed through the low-pass filter from which the imaginary part of the Impedance (Im) is derived, as in Equation (8).

$$v_{LPF90^\circ} = \frac{A_v i_0 Z_x v_0}{2} sin(\varphi + \Delta\theta) \tag{8}$$

$$Im = (sin(\,\varphi + \Delta\theta)) = \frac{2 * v_{LPF90^\circ}}{A_v i_0 v_0} \tag{9}$$

The impedance magnitude derives from the SD system:

$$|Z| = Z_x \sqrt{cos^2(\varphi + \Delta\theta) + sin^2(\varphi + \Delta\theta)} \tag{10}$$

$|Z| = Z_x * 1 \therefore$ *magnitude is unaffected by* $\Delta\theta$

While the phase is obtained as

$$\angle Z_x = tan^{-1}\left(\frac{sin^2(\varphi + \Delta\theta)}{cos^2(\varphi + \Delta\theta)}\right) \therefore \textit{phase measured is ffected by } \Delta\theta \quad (11)$$

Although phase delays between the measured voltage of load impedance (v_{meas}) and I and Q demodulation signals do not significantly impact the magnitude of the measured impedance, they notably affect the precision of the measured impedance phase. Consequently, this result may lead to erroneous assessments and diagnoses in bioimpedance applications that rely on precise detection of the load impedimetric phase.

The block diagram shown in Figure 3 illustrates the SD system block incorporating phase correction methodology proposed in this paper. With switches S2 and S3 closed to com 1 and com 2, respectively, the system functions in a closed-loop system, activating the phase compensation mechanism. The output current (I_{out}) from the current source undergoes constant phase monitoring facilitated by a very low tolerance (Rsense) carbon film resistor integrated into a series with load impedance. The voltage output (Vsense) of Rsense is precisely measured via an Instrumentation Amplifier (IA) placed very close to Rsense, mitigating parasitic capacitance induced by long signal tracks. Subsequently, phase differences between Vsense and the reference sinusoidal voltage (V_{in}) are compared using a Type II phase detector. Phase differences provide a pulse that tunes the phase synchroniser via a microcontroller until an equivalent phase delay is added to the I and Q demodulation signals. This step causes the phase detector pulse to become low and remain low until another phase difference occurs. Vmeas is now multiplied with demodulation signals after phase correction, and low-pass filtered to eliminate AC components. The resultant DC voltages are further analysed after the low-pass filter to obtain real and imaginary components of the impedance and express them in polar form according to Equations (10) and (11).

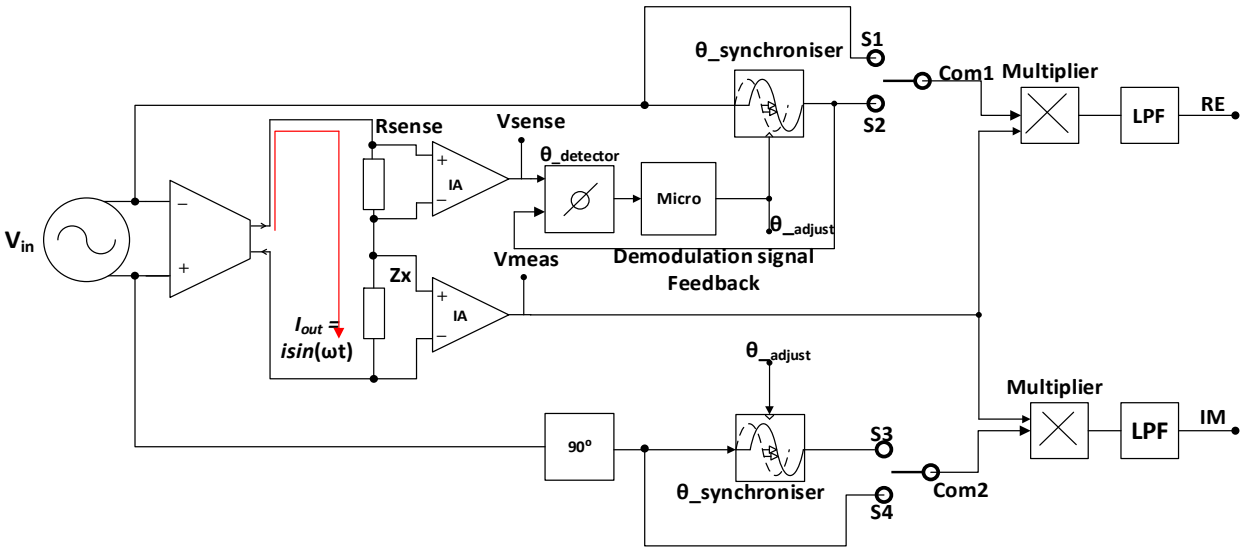

Figure 3. Block diagram of the automatic Phase Error Compensated Synchronous Demodulation system (PECSD).

2.2. PECSD Circuit Design

Figure 4 illustrates the circuit-level implementation of the PECSD, which comprises a Mirrored Enhanced Howland Current Source (MEHCS), a delay block phase synchronizer, a type II phase detector, and a lock-in amplifier.

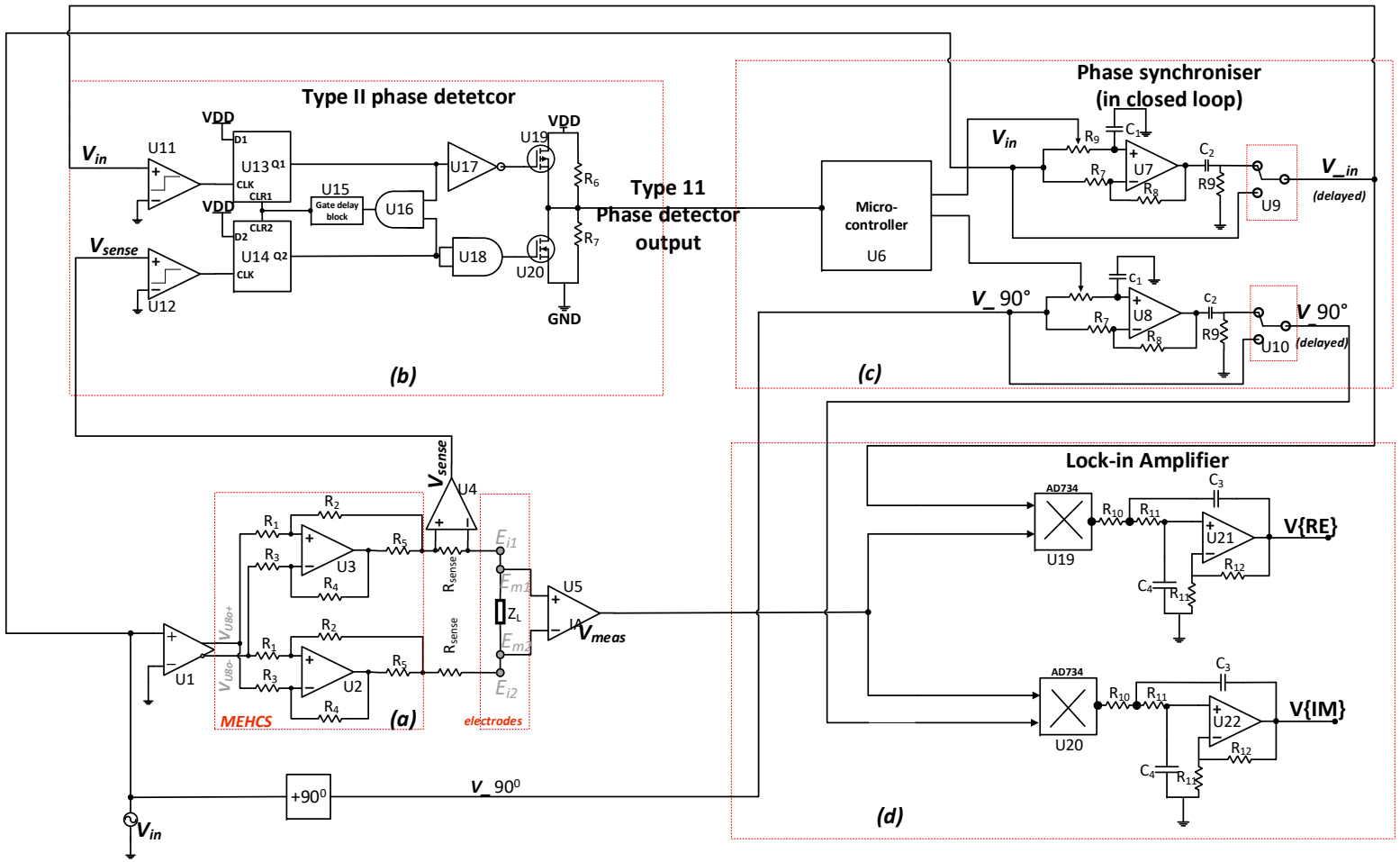

Figure 4. Main circuit stages of the PECSD bioimpedance measurement system. showing (**a**) MECHS (**b**) Type II phase detector, (**c**) Phase synchroniser and (**d**) Lock-in Amplifier.

To implement the phase synchroniser in Figure 4, the current source is driven by U1, a unity gain single to differential op amp that increases common mode rejection and minimises DC offset [26]. The current source consists of U2 and U3 op amp arranged to provide a Mirrored enhanced Howland current source (MEHCS), ensuring true floating load. As such, the output current flowing through the load impedance Zx and sense resistor Rsense is:

$$I_{out} = g_m V_{in} \tag{12}$$

where, g_m is the transconductance of the Howland current source provided by [27].

$$g_m = \frac{R_4}{R_3 * R_5} \tag{13}$$

U4 and U5 are instrumentation amplifiers for measuring the resultant voltages across Rsense and Load. In a closed-loop system, Vsense and V_{in} should ideally be in phase and squared through comparators U11 and U12, respectively. The outputs of U11 and U12 are compared in phase using a type II phase detector involving D-type flip flops U13 and U14 and, subsequently, a delay logic gate U15, which offers just enough delay to overcome FETS U19 and U20 dead zones. U16 simultaneously resets U13 and U14 when the Vsense and V_{in} phases are synchronised. The U13 Q1 output activates a positive charge pump; however, when V_{in} leads, the complimentary U14 Q2 output will also activate a negative charge pump when V_{in} lags Vsense. However, only one of these conditions can occur at a time.

The type II phase detector sends a square pulse to the microcontroller (U6), which detects phase shifts between Vsense and V_{in} and initiates a response to cancel the phase shift between Vsense and V_{in} by delaying V_{in} for an equivalent phase interval. It achieves this by automatically adjusting the wiper of the digital potentiometer of the all-pass filters U7 and U8. The digital potentiometer further stores the wiper's position in its memory once the required phase compensation is achieved. Multiplication is achieved through a lock-in amplifier mechanism comprising U19–U22. The same procedure is performed in the quadrature demodulation cycle.

Tables 1 and 2 provide a detailed illustration of the raw data and output variables pertaining to a 1 kΩ purely resistive load and an RC load consisting of a 1 kΩ resistor and 244 pF capacitor, across a frequency range of 1 kHz–300 kHz. These measurements were obtained for an output current (I_{out}) of 1 mA. Following Equations (10) and (11), it becomes evident that the phase shift compensation between Vsense and the I &Q demodulation signals had minimal impact on the impedance magnitude, as shown in Tables 1 and 2. A significant difference in load impedance phase was noted at higher frequencies before and after phase compensation, as evidenced by the load impedance values before and after phase shift compensation.

2.3. Experimental Setup

The SD system proposed in this paper was tested under various loads and frequencies employing the setup shown in Figure 5a. This arrangement includes a power supply, a signal generator to generate V_{in}, an oscilloscope, and a DAQ module for data transmission to the PC. The experiments were conducted with both resistive and capacitive loads. Figure 5b also provides a photograph of the SD system with phase compensation on the printed circuit board, highlighting its key stages.

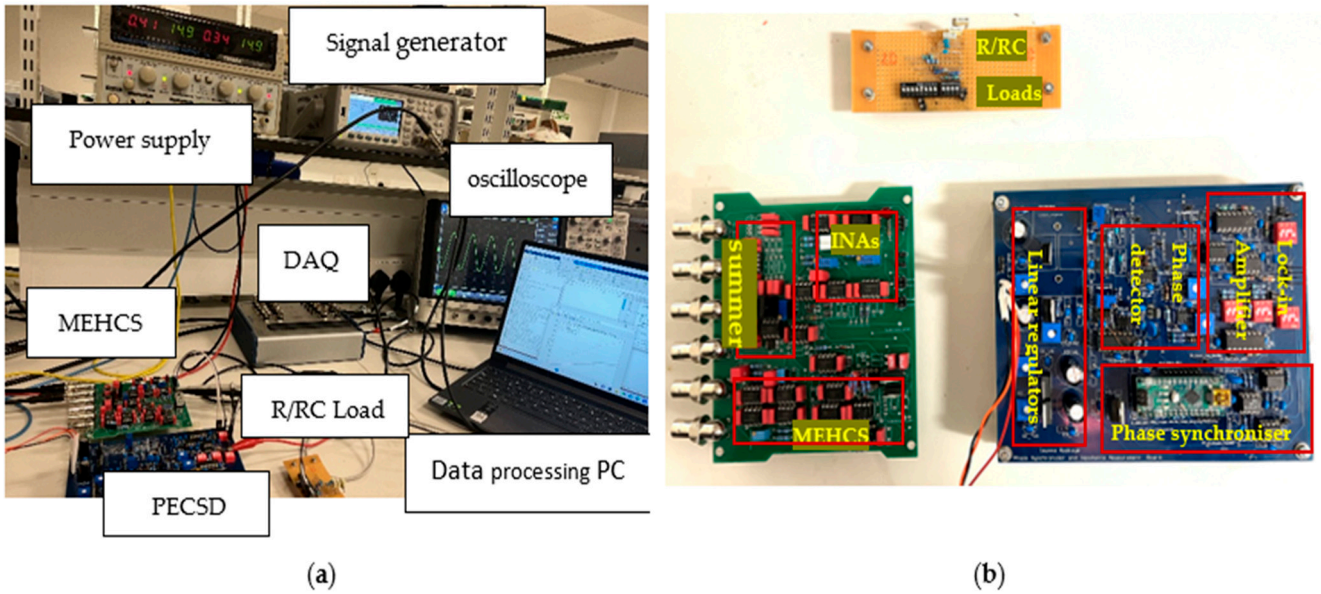

Figure 5. (**a**) Picture of experimental setup; (**b**) picture of circuit board.

Tables 1 and 2 below further illustrate the impedance output variables for both phase-compensated and uncompensated synchronous detection systems for resistive loads, as well as resistive and capacitive loads.

Table 1. Impedance output variables for both phase compensated and uncompensated synchronous detection system. *R Load = 1* kΩ, *Rsense* = 1 kΩ. *IA gains:* A_{Vsense} = 1, A_{Vmeas} = 1. I_{out} = 1 mA. V_{in} = 1 V.

	Table of Resultant Impedimetric Values for 1 KΩ across a range of Frequencies, Comparing SD with and without Phase Compensation (Figure 7).				
Load	**Frequency**	**$\lvert Z_x \rvert$ with Phase Compensation**	**$\lvert Z_x \rvert$ W/O Phase Compensation**	**φ with Phase Compensation**	**φ W/O Phase Compensation**
R = 1 kΩ	1000	997.77	986.30	1.47	1.64
	10,000	996.32	986.13	1.03	1.27
	100,000	961.95	957.70	1.68	11.10
	200,000	891.03	880.59	0.12	18.86
	300,000	818.70	826.89	4.04	23.39

Table 2. Impedance output variables for both phase compensated and uncompensated synchronous detection system. *R Load* = 1 kΩ, *RC Load* = 1 kΩ + 244 pF. *Rsense* = 1 kΩ. *IA gains:* A_{Vsense} = 1, A_{Vmeas} = 1. I_{out} = 1 mA. V_{in} = 1 V.

	Table of Resultant Impedimetric Values for RC Load of 1 KΩ and 244 pF Across a Range of Frequencies, Comparing SD with and without Phase Compensation (Figure 9).						
Load	**Frequency**	**$\lvert Z_x \rvert$ Ideal**	**$\lvert Z_x \rvert$ With Phase Compensation**	**$\lvert Z_x \rvert$ W/O Phase Compensation**	**φ Ideal**	**φ with Phase Compensation**	**φ W/O Phase Compensation**
RC = 1 kΩ & 244 pF	1000	999.99	991.54	986.23	0.08	1.85	1.48
	10,000	999.88	991.92	988.64	0.87	2.44	3.12
	10,0000	988.46	974.38	973.84	8.71	9.31	18.81
	20,0000	956.10	838.78	844.15	17.03	15.96	33.35
	30,0000	908.59	752.30	746.28	24.68	22.01	43.67

3. Experimental Results

3.1. Phase Error Detection before and after Compensation

Figure 6a,b shows the phase compensation mechanism used in the proposed system outlined in this paper. To showcase the error phase, measurements were obtained before and after phase compensation.

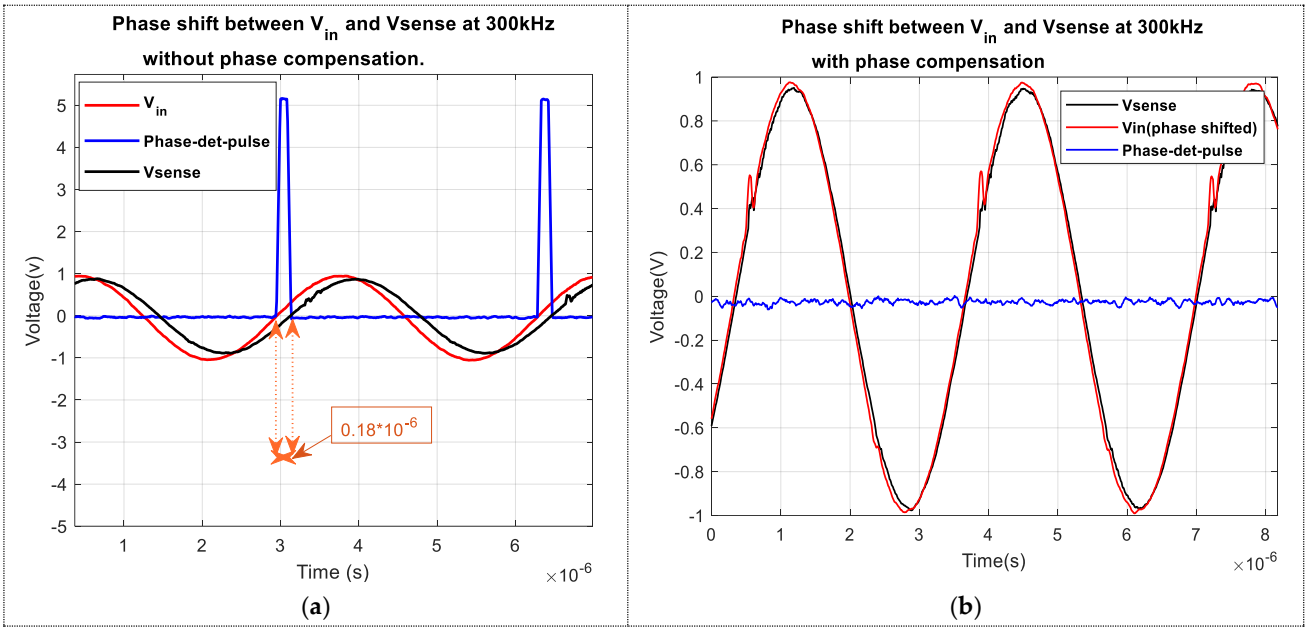

Figure 6. Vsense and V_{in} before and after phase compensation. (**a**). Phase shift between Vsense and V_{in} at 300 kHz before phase compensation. (**b**). Phase shift between Vsense and V_{in} at 300 kHz after phase compensation.

The output of the type II phase detector Phase-det-pulse generates a pulse of 0.184 µs at 300 kHz. This pulse corresponds to the phase difference between the demodulator signal V_{in} and the measured signal Vsense. Accordingly, applying Equation (14), this pulse width corresponds to an erroneous phase shift of approximately 19.44°.

$$\theta = \Delta t * f * 360 \tag{14}$$

where, f is the frequency of V_{in}.

This value has significant clinical implications. In applications where tissue phase values serve as critical diagnostic indicators, as in cancer and bioelectrical impedance myography, a misinterpretation of such a substantial phase shift could lead to potential misdiagnoses and potentially endanger the patient [28]. Diagnostics must be interpreted with utmost precision and caution.

However, with phase compensation feedback activated, it is worth mentioning that V_{in} is delayed until in phase with Vsense. At this point, the Phase-det-pulse settles to zero, indicating no phase error between V_{in} and Vsense, as illustrated in Figure 6b.

Figure 7a shows the impedance magnitude for various resistive loads and their respective percentage errors in Figure 7b. Notably, the bandwidth consistently measures 10 kHz for all loads, beyond which the circuit performance degrades, particularly at loads greater than 1 kΩ. It is worth highlighting that phase compensation has minimal effects on the SD system's impedance magnitude.

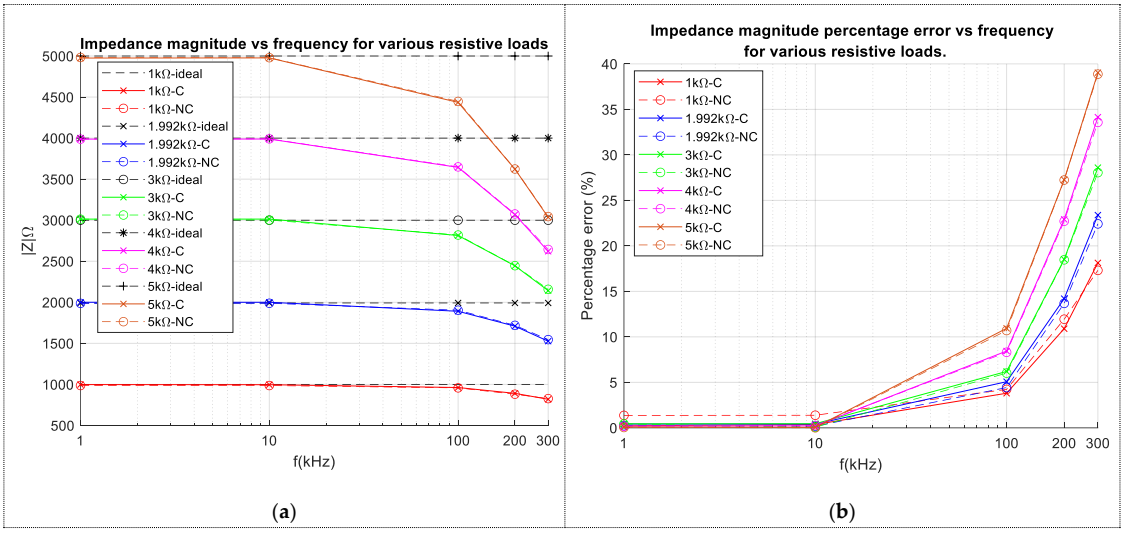

Figure 7. (**a**) Impedance magnitude vs. frequency for resistive loads. C = compensation; NC = No compensation. (**b**) Impedance magnitude percentage error vs. frequency for resistive loads. C = compensation; NC = No compensation.

Figure 8 demonstrates a considerable enhancement in phase error correction, particularly at higher frequencies. In the absence of compensation, a resistive load of 5 kΩ at 300 kHz exhibited significant phase errors of up to 38°. Though the frequency here exceeded the optimal bandwidth limit of operation for this system at loads greater than 1 kΩ and frequencies greater than 10 kHz, as seen in Figure 7a, it stands in contrast to the significantly reduced phase error of 17° observed in the SD system with compensation applied for the same load and frequency.

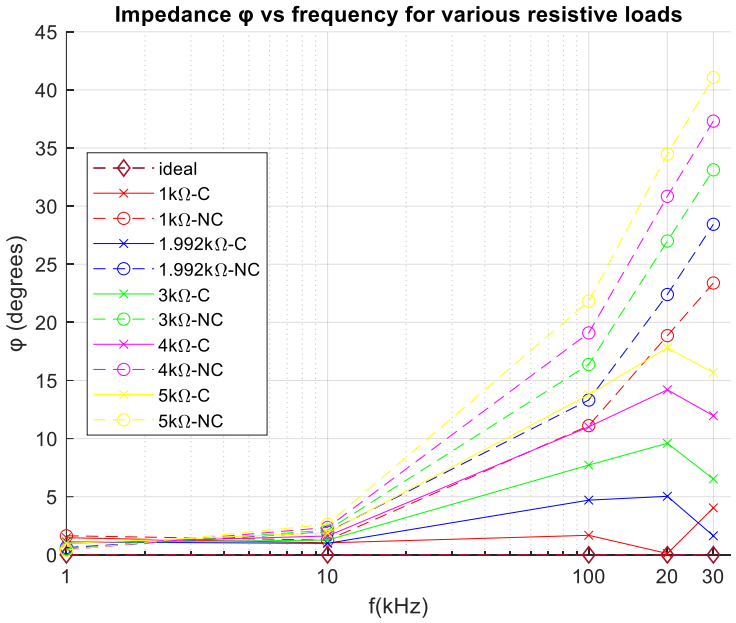

Figure 8. Impedance phase errors for compensated and uncompensated SD systems as a function of frequency for resistive loads.

While achieving the ideal correction of an erroneous phase shift to 0° is theoretically desirable, it may prove challenging for resistive loads due to the potential difficulty in attaining a zero imaginary output from lock-in amplifiers. The reason for this may be mixer-induced errors in the form of differential lags between inputs and offsets [22,29,30].

3.2. Frequency Response

Figure 8 further justifies the phase difference observed between the measured signal Vsense and demodulation signal V_{in}, as in Figure 6a, for a load of 1 kΩ and frequency of 300 kHz. Whilst the phase difference observed in Figure 6a is about 19.44°, as calculated from the phase detector pulse width, the erroneous phase observed in Figure 8 for 1 kΩ was notably 23°. As such, the additional phase difference of 4° may be due to non-idealities of the lock-in amplifier.

Figure 9a,c showed the impedance magnitude as a function of frequencies for RC loads of (1 kΩ, 244 pF) and (3 kΩ, 33.5 nF), respectively. Figure 9a,c shows no significant improvement with phase compensation unlike the counterpart figures in Figure 9b,d, which showed significant improvement in phase error correction. The percentage phase errors for Figure 9b,d were further illustrated in Figure 10b, where the SD system without compensation for RC loads of (1 kΩ, 244 pF) and (3 kΩ, 33.5 nF) exhibited phase errors of approximately 19% and 21% at 300 kHz, respectively. After phase compensation, however, they were significantly reduced to 2° and 4%. These findings underscore the critical role of phase compensation in enhancing accuracy. The clinical significance of these phase errors becomes evident considering previous research [28], where phase differences between healthy and cancerous tissues were approximately 20°, 17°, and 11° at frequencies of 100 kHz, 200 kHz, and 300 kHz, respectively. As such, without proper phase correction, there is a substantial risk of diagnostic unreliability, potentially leading to misidentifying healthy tissue as cancerous. Therefore, accurate phase compensation in diagnostic procedures using SD systems is needed.

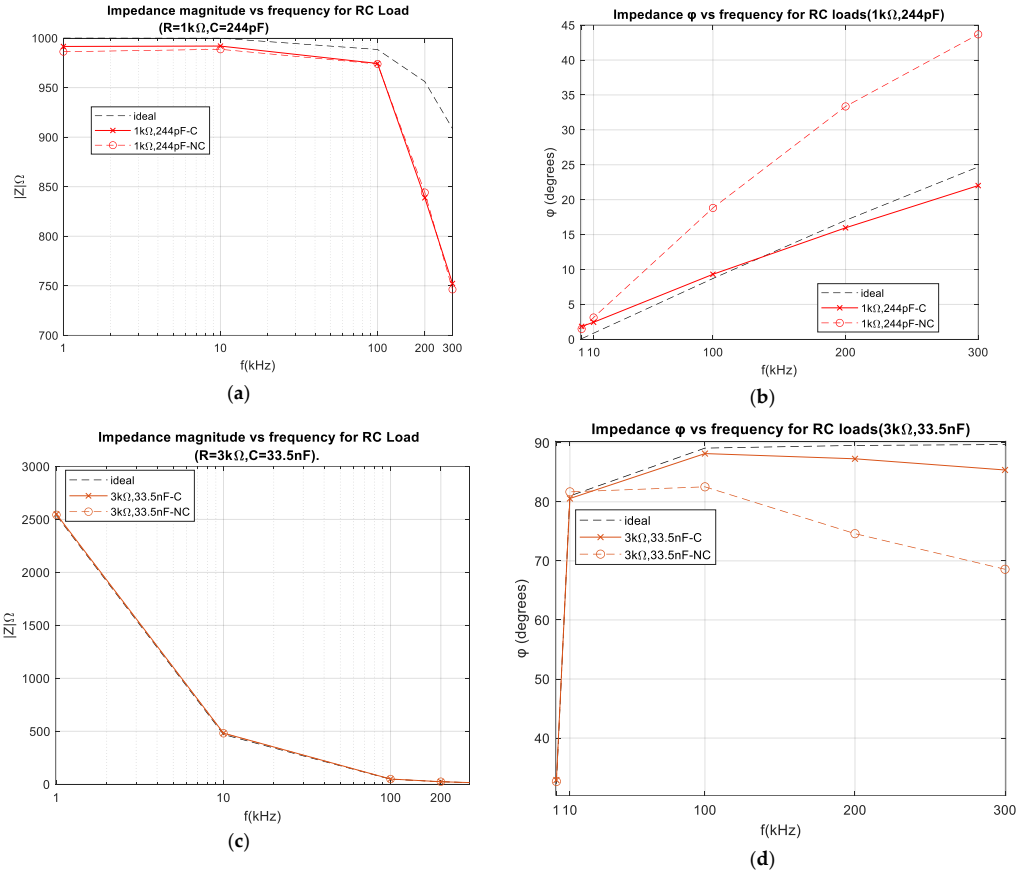

Figure 9. Impedance magnitude and phase for RC load (3 kΩ, 33.5 nF) as a function of frequency. (**a**) Impedance magnitude for RC load (1 kΩ, 244 pF) as a function of frequency. (**b**) Impedance phase for RC load (1 kΩ & 244 pF) as a function of frequency. (**c**) Impedance magnitude for RC load (3 kΩ, 33.5 nF) as a function of frequency. (**d**) Impedance phase for RC load (3 kΩ, 33.5 nF) as a function of frequency.

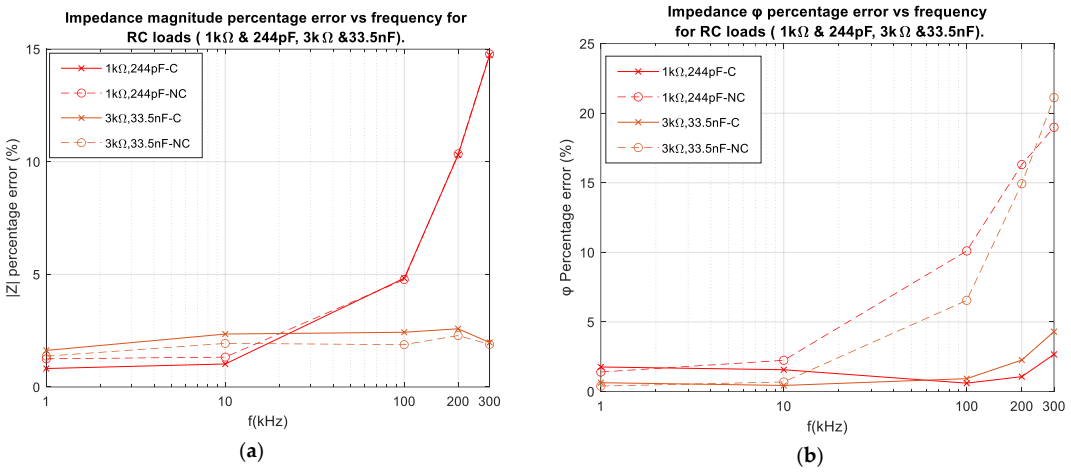

Figure 10. Impedance magnitude and phase percentage error for RC loads as a function of frequency. (**a**) Percentage impedance magnitude error for RC loads. (**b**) Percentage phase error for RC loads.

3.3. Settling Time

Figure 11a,b shows the settling time for conventional SD systems and SD systems with phase compensation, respectively. The response time of conventional SD systems predominantly relies on the settling time of filters used in the output stages. SD with phase compensation exhibits a slightly longer response time with step changes in input voltage amplitude. The reason for this is that the final settled value of output low-pass filters depends on the time required by the all-pass filter to add an adequate delay to synchronise the sense voltage Vsense with the demodulation signals in phase.

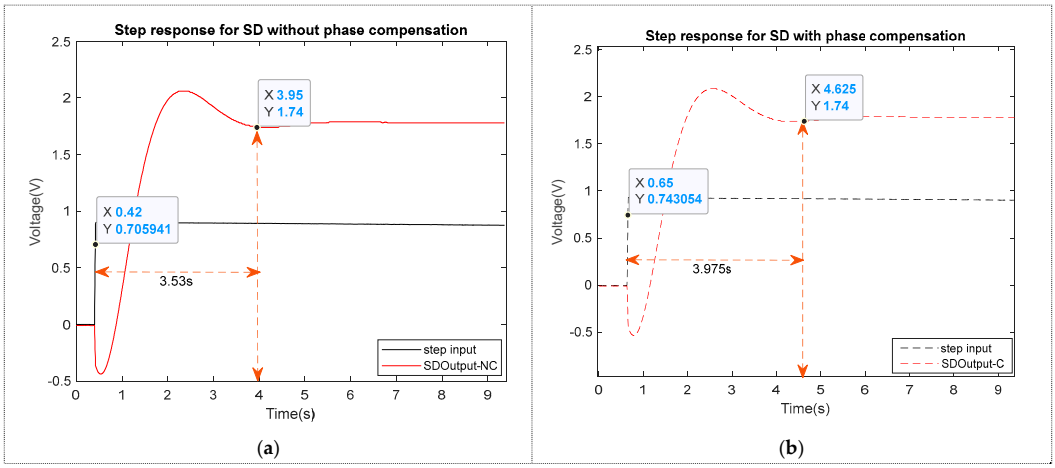

Figure 11. System step response. (**a**) Step response for SD system without phase compensation. (**b**) Step response for SD system with phase compensation.

The system's settling time at 1 kHz with a typical load of 4 kΩ was monitored by capturing the output of the low-pass filter at a step input of 0.9 V. Settling time was measured as the time required for the system to settle at 97% (1.74 V) of the final expected value of 1.8 V for a filter gain of 2. The SD system with phase compensation was 445 ms slower than without compensation. This difference may not be a significant concern for most bioimpedance applications, where the measured impedance is relatively slow, varying with applications where specific frame rate requirements are required for multiple channel recordings, as in electrical impedance tomography [3,31].

4. Simulations

Frequency Response

To validate these experimental findings, simulations were conducted for both purely resistive loads and RC loads. Figure 12a,b presents the impedance magnitude percentage error and its corresponding phase errors for resistive loads of 1 kΩ, 3 kΩ, and 5 kΩ. These graphs highlight the negligible effects of erroneous phase shifts between VCCS and I &Q demodulation pulses on the impedance magnitude, unlike the phase.

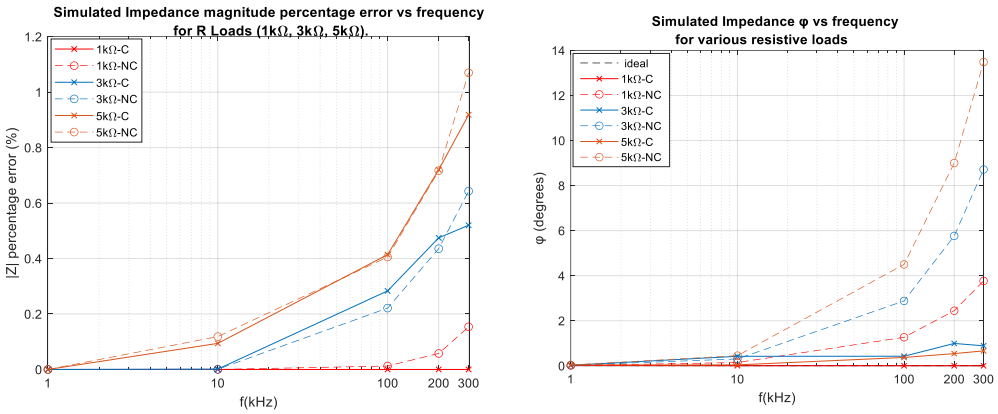

Figure 12. Simulated Impedance magnitude and phase errors for RC Loads as a function of frequency. (**a**) Simulated Impedance magnitude percentage error for phase compensated and uncompensated SD systems as a function of frequency for R = 1 kΩ, 3 kΩ, and 5 kΩ. (**b**) Simulated impedance phase error for phase compensated and uncompensated SD systems as a function of frequency for resistive loads.

This observation is true for both compensated and uncompensated systems, with a percentage error difference of $\leq$1.2% across all loads. However, a phase error differential of over 12°was observed between the compensated and uncompensated SD system for a 5 kΩ load, as shown in Figure 12b, which significantly impacted the impedance phase accuracy.

Figure 13a,b also shows percentage errors for both the impedance magnitude and phase before and after compensation for RC loads of (1 kΩ, 244 pF) and (3 kΩ, 33.5 nF), respectively. Both results showed lower errors unlike the experimental data, which might be attributed to simulations' lack of consideration for realistic experimental factors, including the non-idealities of certain components, i.e., leads, connectors terminals, and printed circuit boards. Results further proved improvement made by phase compensation.

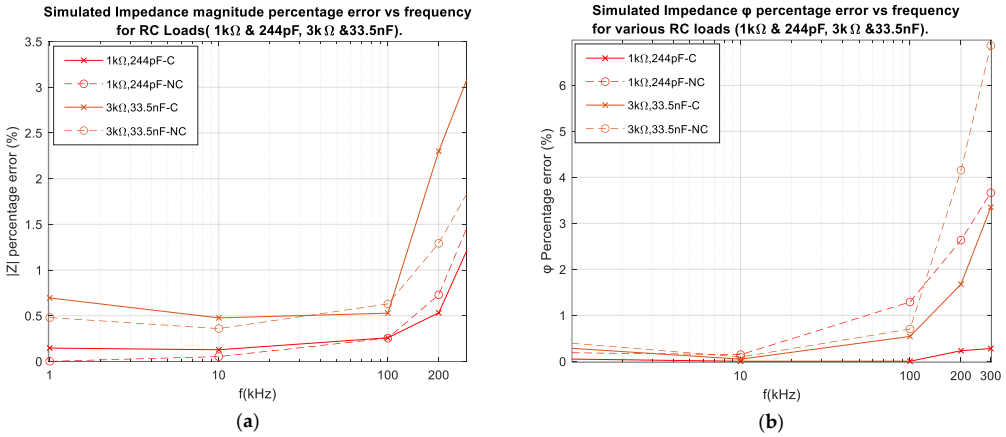

Figure 13. Simulated impedance magnitude and phase percentage error for RC loads as a function of frequency. (**a**) Simulated impedance magnitude and percentage error as a function of frequency for RC loads. (**b**) Simulated impedance and phase percentage error as a function of frequency for RC loads.

5. Performance Overview

5.1. Noise

At low frequencies, operational amplifier noise spectral density rises to 3 dB/octave. The power spectral density in this region is inversely proportional to frequency; therefore, the voltage noise spectral density is inversely proportional to the square root of the frequency and is commonly referred to as $\frac{1}{f}$ noise [32,33]. Since the output of a synchronous demodulator is a DC signal, it is prone to excessive flicker ($\frac{1}{f}$) noise, as provided by Equation (15).

$$\frac{1}{f} = efnorm\sqrt{\ln\left(\frac{f_H}{f_L}\right)} \tag{15}$$

where, $efnorm$ is the normalised value of noise voltage spectral density in the $\frac{1}{f}$ region; f_H is the upper cut-off frequency; f_L is the lower cut-off frequency corresponding to 0.1 Hz.

To avoid an increase in flicker noise due to compensation, the output of the phase synchroniser circuit was high-pass filtered at a cut-off frequency of fc = 16 Mhz, which is over five decades more than the signal bandwidth to avoid affecting both the amplitude and phase of demodulator signals. To further verify this effect, noise analysis was performed on Lt spice for SD systems with and without compensation. The outcome remained the same in both cases, as illustrated in Figure 14.

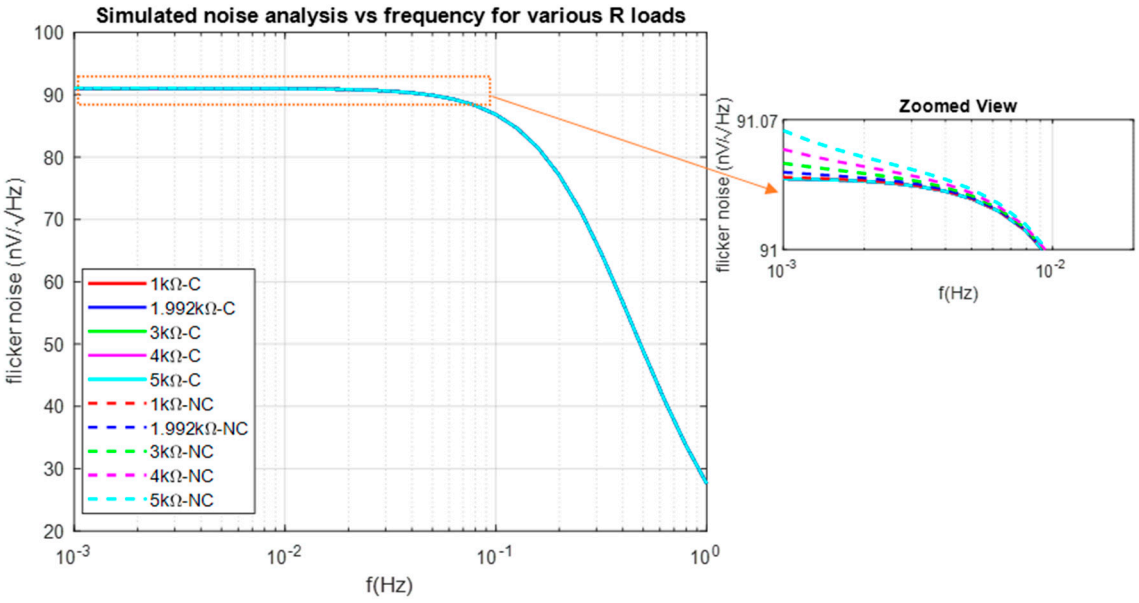

Figure 14. SD noise analysis with and without phase compensation.

5.2. Effects of Sense Resistor R_{sense} Phase Error on Measurement Accuracy

We also modelled the sense resistor R_{sense} using an equivalent circuit with data from the datasheet to determine the effect of its parasitic components on the measured signal phase at the system's maximum bandwidth. Rsense is a high-precision 1 KΩ Foil Resistor with a TCR of ±2.0 ppm/°C and a tolerance of ±0.005% according to the datasheet [34]. It has a maximum parasitic capacitance and inductance of 1 pF and 0.1 uH, respectively. The equivalent circuit is illustrated in Figure 15.

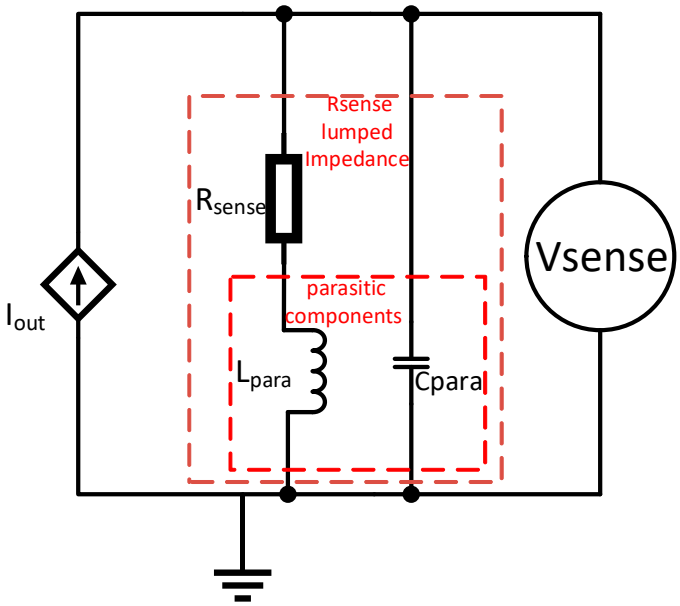

Figure 15. Rsense Lumped Impedance model.

Figure 15 illustrates the lumped impedance model of Rsense, which was used to determine phase error contribution to the overall measured phase. The model was tested at the highest bandwidth specified in this paper. The corresponding phase contribution of these values is below 0.03°, which is negligible.

Another source of error relates to the common mode signal component of the differential voltage across Rsense. This error type can alter the comparator response and, thus, phase detection. Using a high CMRR instrumentation amplifier eliminates that error across the spectrum.

Table 3 further shows a summary of measured performance of PECSD.

Table 3. Summary of PECSD measured performance.

Architecture	Discrete
PCB Active area	130 mm × 162 mm
Supply Voltage	±15 V
Bandwidth	1 kHz–300 kHz
Phase Measurement accuracy	
% Error of Experimented RC loads @ full bandwidth.	≤5% with phase compensation ≤21.1% without phase compensation
Settling time @ 98% of final value	3.965 s with phase compensation 3.53 s without phase compensation
Maximum output generated noise	91 nv/Hz with and without phase compensation

6. Conclusions

In this study, we introduced a Phase Error Compensated Synchronous Demodulation system (PECSD), a discrete component realization of the SD bioimpedance system featuring automatic phase error correction. Our work focused on eliminating a fundamental, systematic, and often unreported source of errors in bioimpedance measurement systems, particularly in phase shifts between the VCCS output current and I,Q demodulation signals in the Synchronous Demodulation/Detection (SD) architecture.

The developed phase compensation method features an auto-adjustable delay block with an all-pass filter. The PECSD system achieved a substantial reduction in phase error at ≤5% across all RC loads compared with the uncompensated SD system, where errors

could reach up to ≤21.1%. This improvement in measurement accuracy will significantly improve SD systems' applicability to diagnostic applications, particularly in scenarios where tissue phase values serve as crucial diagnostic indicators, such as in cancer diagnosis and bioelectrical impedance myography. This system applies to a wide range of applications beyond bioimpedance (e.g., electrical impedance spectroscopy or tomography), and works for a wide range of loads. Specific loads were chosen for their relevance to specific biomedical applications (e.g., skin cancer and other skin conditions, i.e., rubor [2,35]) and because 1–5 kΩ load values are used in the vast majority of bioimpedance instrumentation research literature [27]. Moreover, with SD impedimetric instrumentation being widely applicable beyond bioimpedance, e.g., electrical impedance tomography and electrochemical impedance spectroscopy, this work is expected to have a wider impact on more accurate electrical impedance sensing systems.

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